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Triangulating BGA Faults with Boundary Scan

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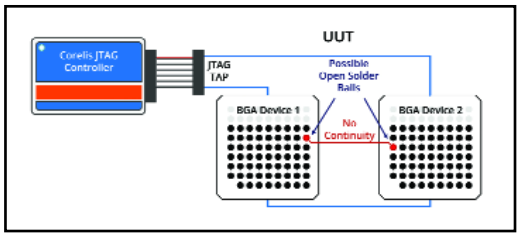
Visual inspection and electrical testing can be highly successful at identifying board-level defects after assembly, but sometimes detection alone is not enough. Today's fine-pitch ball grid array (BGA) devices, in particular, present real problems. There is often no physical or visible access to the device pins, limiting diagnostic capability. Even when an open circuit is detected between two BGA devices, this data alone is not enough to determine which device is actually at fault. Even X-ray inspection equipment cannot always provide conclusive visual evidence when such a defect is encountered.



JTAG testing can be used to identify faults between BGA boundary scan devices.

Fault Detection with JTAG

When it comes to structural testing of printed circuit board (PCB) assemblies that include BGA devices, JTAG is a preferred test method since it is not reliant on physical access to each pin. Since BGA packaging does not offer direct physical access to external probes, this makes using external probe methods, such as in-circuit test (ICT) and flying probe testing, ineffective.

In JTAG devices, the test circuitry resides inside the chip itself and is controlled by the JTAG test access port (TAP) — a simple five-wire interface. Using this circuitry, boundary scan allows physical pins on the chip to become JTAG test points. This is decisively different from external probes that physically access test points on the unit under test (UUT).

During a JTAG test, one JTAG-compliant BGA device drives test patterns on its pins, while a second JTAG-compliant BGA device verifies the expected pattern on corresponding pins. When the patterns match, it means that there is continuity between the pins. If we expect continuity to exist between the two pins and the test patterns do not match, then there is likely a defect present. Even if JTAG tests can correctly identify the defect as an open circuit, they cannot isolate which device has the open pin, even if the driver and receiver are swapped. Without knowing exactly which device is causing the fault, repair work can turn into a 50/50 guess for technicians, resulting in unnecessary repairs.

Isolating and Diagnosing Faults

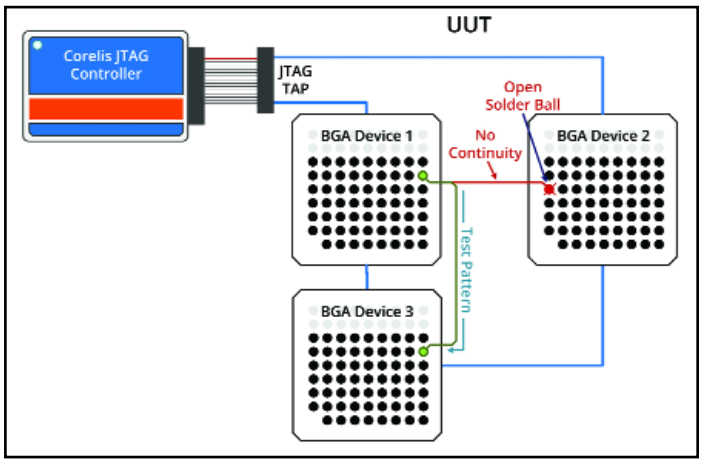
Ideally, a third JTAG pin in the circuit will be available to assist in fault isolation. For example, if one BGA pin is open due to an assembly fault, a pin on the third JTAG-compliant BGA device would be able to confirm continuity to the good BGA pin. The remaining pin, which still cannot be confirmed for continuity, represents the faulty device. With this additional information, it is easy to identify the likely fault as an open solder ball and isolate repairs to just the faulty BGA device.

Not all circuits will include more than two JTAG pins and, even in cases of three or more pins, the additional pins might not offer JTAG control. In these cases, it is possible to externally attach a general-purpose IO (GPIO) pin from the JTAG controller to the circuit using a passive component, test point, via, or the actual trace itself. If the driving BGA pin makes a successful connection, the GPIO pin will receive the expected test pattern when JTAG test vectors are applied. If the driving BGA pin does not make a connection (open fault), the GPIO pin will not receive the expected test pattern when JTAG test vectors are applied, indicating a lack of continuity. This way, the fault can be pinpointed to a single pin.

JTAG Starter Kit

Corelis offers a JTAG starter kit, which is a toolset with everything required to isolate the problem when BGAs have an open fault. The kit includes a variety of tools and features to control and observe system signals of a boundary scan com-

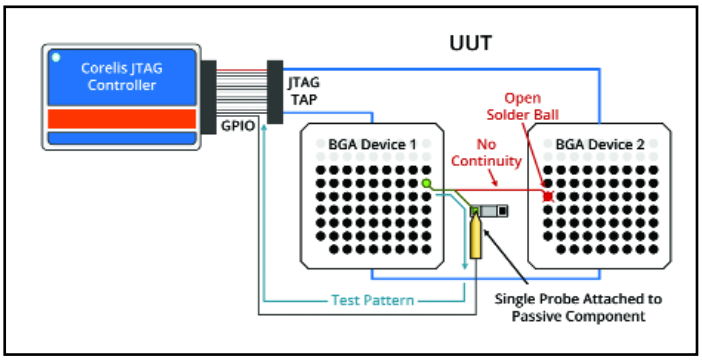
patible UUT. The included USB 2.0 controller allows JTAG commands to be executed from any Windows-based PC and provides convenient GPIO circuitry that can be utilized as



Faults can be diagnosed to a single pin with three interconnected BGA boundary scan devices.

additional measurement pins to help isolate open failures between BGA pins. Other useful features of the JTAG starter kit include:

- Interactive, real-time visual control and observation of all JTAG-controllable input and output signals.
- Basic and advanced scripting modules that provide powerful, automated access to JTAG signals.
- A JTAG protocol command module for direct low-level access to JTAG scans.
- A maximum TCK rate finder for optimizing JTAG test speed.
- Opcode discovery to identify potential undocumented instructions on each JTAG device.
- SVF, JAM and STAPL file programming.
- Netlist conversion support for a wide variety of CAD vendors.



BGA open faults can be diagnosed to a single pin using a combination of JTAG and a GPIO pin.

- Customizable graphical user interface (GUI) with window docking.
- Powerful API interfaces for easy integration with popular third-party test executives.

With boundary scan testing, it is possible to detect faults that can not be identified with test methods that require physical access. Using three JTAG pins in a circuit, defects can be quickly and easily triangulated and identified.

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