



CVXI-1149.1
VXIbus BOUNDARY SCAN
CONTROLLER BOARD

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USER'S MANUAL

P/N UM00090001-A2

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Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software code may be printed before the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

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About this Chapter

This chapter introduces you to the CVXI-1149.1 Boundary Scan Controller module. The main sections of this manual are:

- Introduction
- What is IEEE-1149.1?
- Brief Product Review

Note: The CVXI-1149.1 is available as a "B" size module as well as a "C" size module. Unless otherwise specified, this manual describes the features of both versions which are functionally identical and differ by their physical dimensions only.

Introduction

The CVXI-1149.1 VXIbus Boundary Scan Controller Board provides an interface between the VXIbus and any JTAG compatible target. The CVXI-1149.1 is designed to control the operation of an IEEE standard 1149.1 (JTAG) test access port by generating the proper signals under software control to interface with the target devices. Up to six test access ports can be controlled, each connecting the CVXI-1149.1 card with a four signal cable to the boundary scanned target system. By controlling the JTAG bus, boundary scan operations per IEEE-1149.1 can be invoked by software. The user is able to command target circuitry Built-In-Self-Test (BIST), verify PCB interconnects, perform functional testing, and debug without the need for manual probing. Furthermore, device internal functions that are not accessible to external probing can be accessed through the JTAG interface, enabling fault isolation within the device itself. A picture of the CVXI-1149.1 is shown in figure 1-1.

Figure 1-1 CVXI-1149.1 Module

What is IEEE 1149.1?

The IEEE 1149.1 test bus and boundary scan architecture allows an IC, and similarly a board or system, to be controlled via a standard four-signal interface. Each IEEE 1149.1 compliant IC incorporates a feature known as boundary scan that allows each functional pin of the IC to be controlled and observed via the four-wire interface. Test, debug, or initialization patterns can be loaded serially into the appropriate IC(s) via the IEEE 1149.1 test bus. This allows IC, board, or system functions to be observed or controlled without actual physical access.

The IEEE 1149.1 test bus is comprised of two main elements: a Test Access Port (TAP), which interfaces internal IC logic with the external world via a four-signal (optionally five-signal) bus as shown in Figure 1-2; and a boundary scan architecture, which defines standard boundary cells to drive and receive data at the IC pins. The IEEE 1149.1 specification also defines both mandatory and optional opcodes and test features. The test bus signals are: Test Clock (TCK), Test Mode Select (TMS), Test Data In (TDI), Test Data Out (TDO), and the optional Test Logic Reset (TRST).

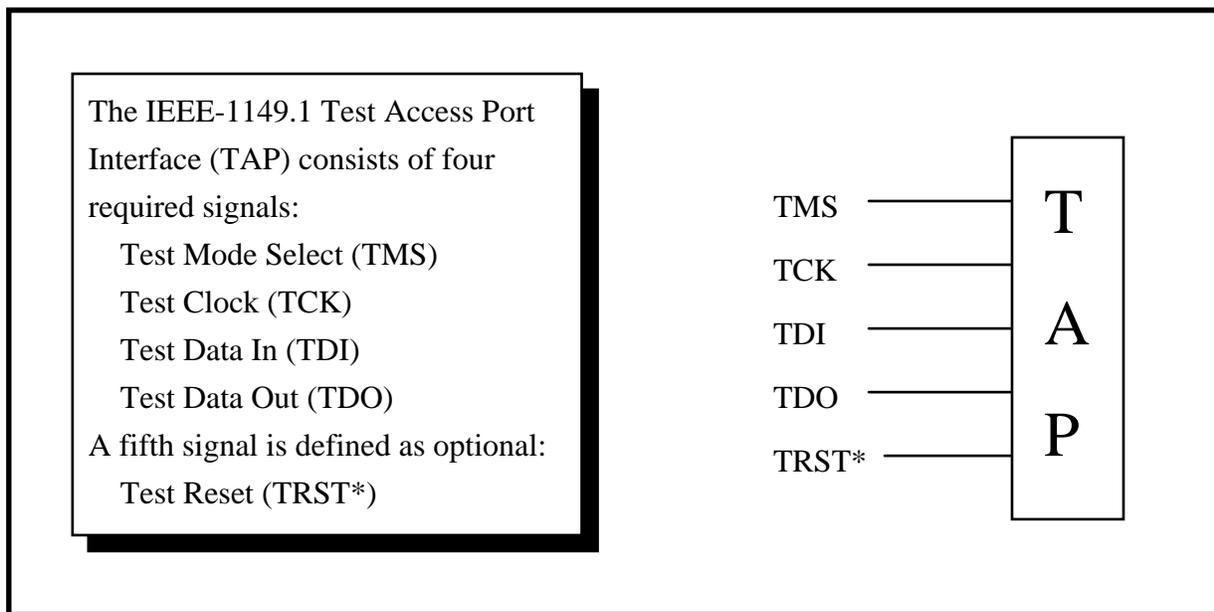


Figure 1-2 Test Access Port (TAP)

Brief Product Review

The CVXI-1149.1 Boundary Scan Controller block diagram is shown in Figure 1-3. It is designed to control the operation of an IEEE Standard 1149.1 (JTAG) scan test path by taking commands from the host computer and generating the proper signals to interface with the target device(s). The host computer can be an embedded VXIbus computer or an external host that controls the VXI chassis via a VXIbus slot 0 controller. The target(s) can be moved from any stable state to another stable state, loaded with instructions, and resulting test data scanned out to be read by the Host. Four EVENT pins are provided to allow real-time interaction between the CVXI-1149.1 and its target(s). The EVENT pins can be configured to generate VXIbus interrupt requests and/or assert TTL triggers whenever a user-definable condition is present.

A 32-bit counter can be preset to allow a predetermined number of clock cycles or instruction executions to occur and can be programmed to set an interrupt flag when it reaches a count of zero.

The CVXI-1149.1 implements all the low-level functions, enabling the host to use higher-level abstraction such as states of IEEE Standard 1149.1 for control, variables indicating command finish, buffer full or empty for status, and strings and buffers for data.

The CVXI-1149.1 may connect without external logic to six parallel chains of IEEE Standard 1149.1 targets, each with its own separate TMS signal. The parallel chains share one or two TDI signals, one TDO signal, and one TRST signal and TCK signal.

The CVXI-1149.1 has four event detectors and two 16-bit event counters to support asynchronous functions. The CVXI-1149.1 can connect to the target via a re-timed link with up to 31 bits of delay. This may be required when the clock rate is high and either the target is at a distance or the link involves fanout or buffer/driver devices.

The CVXI-1149.1 is an A16/D16 VXIbus slave device and interrupter with a 16-bit data bus. The critical VXIbus interface timing is independent of the JTAG clock period.

The major functions of the CVXI-1149.1 are controlled by specific commands:

The **STATE** command controls the target interface and target state diagrams. It can change the current state to any stable state.

The **EXECUTE** command causes the target to execute instructions that have been shifted into it. It uses the Run-Test/Idle state, and can execute instructions for a fixed time or until an event occurs.

The **SCAN** command circulates data among targets and transfers data between the CVXI-1149.1 and targets. It uses the Shift-IR or Shift-DR states, and also the read and write buffers.

Figure 1-3 CVXI-1149.1 Block Diagram

Programmable Clock

The CVXI-1149.1 card TCK clock output to the JTAG compatible target system is programmable by user software. The user is able to select either an internal on-board XTAL oscillator or an external target supplied clock.

The internal clock circuitry includes a programmable clock divider and pre-scaler logic. Any one of sixteen different divide values, from divide by 2 to divide by 32, can be selected. A pre-scaler of divide by 1 or divide by 32 can also be selected. Using the on-board 25 MHz crystal oscillator, 32 different TCK rates ranging from 24.4 KHz to 12.5 MHz are user selectable.

If other clock rates are required, the user can select the external clock source and provide the clock signal from either another VXIbus instrument or from the target system. Optionally, the user can install his own crystal oscillator chip into the crystal oscillator socket that is provided on the CVXI-1149.1 card.

A single-step mode is also provided to enable the user to fully control the TCK signal high and low states. When the single step mode is selected, the external clock source and the on-board crystal oscillator are not used. Instead, the software write operations to the appropriate bit in the COMMAND register toggle the TCK signal and result in a user controlled clock signal. The programmer is able to single-step through the JTAG environment in a fully static mode of operation. This feature is very useful for debugging software drivers and integrating complex JTAG compatible test systems.

Parallel Input/Output Ports

The board contains 32 TTL compatible parallel inputs and 32 TTL compatible parallel outputs. The input and output signals are organized into 16 bit parallel ports. Each of the parallel input and output ports are directly accessible by the host computer by reading or writing the appropriate VXIbus A16 register.

The 32 parallel outputs are driven by four tri-state octal buffers, with 8 outputs per buffer. The outputs of each of the buffers can be put into tri-state under software control. The command register includes four Output Enable bits, each of which controls one octal output buffer.

The input and output ports can be used to control and sense various non-JTAG functions in the target system. These ports are useful for testing of target systems that incorporate a mixture of JTAG and non-JTAG compatible hardware.

JTAG Compatible Logic

The CVXI-1149.1 contains two JTAG compatible 74BCT8244 octal buffers that are connected in parallel with the TTLTRG Trigger Input Select Register, which is one of the on-board A16 registers. The serial test busses of the 74BCT8244 devices are daisy chained and then connected to the first set of on-board serial test busses.

In normal mode of operation, these devices can be used as read-back buffers. Data written to the Trigger-In select register port can be read-back from the particular A16 register assigned to these octal buffers. In the diagnostic mode, the normal operation of the octal buffers is inhibited and the Test Access Port circuitry is enabled to scan the device's I/O boundary.

The user can program the Trigger-in Select register with arbitrary data, and then read it back via the JTAG serial interface to verify that the data scanned matches the actual data presented at the buffer input pins.

This feature provides extensive self-test capabilities on the CVXI-1149.1 board and enables the user to exercise his software and test this "simple" JTAG compatible circuitry before attempting to connect to more complicated target systems.

Interrupts and Triggers

The SN74ACT8990 test bus controller INTR interrupt request signal can be configured by the user to drive one of the seven VXIbus interrupts and/or one of the eight VXIbus TTLTRG trigger lines. The INTR signal is a programmable interrupt request that is set by external event signals and/or internal SN74ACT8990 conditions. Refer to the SN74ACT8990 application note in Appendix B for additional details regarding the operation of the INTR signal and the various programming options for this powerful feature.

The use of interrupts and triggers is an important feature for synchronizing the target system with the CVXI-1149.1 card and for synchronizing multiple VXI modules, including multiple CVXI-1149.1 cards. EVENT signals can detect an asynchronous event in the target system and consequently start or stop serial JTAG data transmission or reception. External events can also be programmed to generate an interrupt request to the host computer or trigger multiple VXIbus modules.

Front Panel

The front panel contains three LED indicators and two connectors. The front panel is shown in Figure 1-4.

The **RESET** amber LED indicates that the JTAG TRST* signal is asserted.

The **EXT CLK** green LED indicates that an external JTAG clock source is being used.

The **SLF TST** green LED indicates that the target interface is in tri-state mode and that the on-board loop-back option is selected (usually during self-test).

The TAP connector is a 40-pin 3M type connector that contains all the JTAG related interface signals. The PIO connector is a 96-pin DIN connector that contains the 64 digital parallel I/O signals.

VXIbus A16 Registers

Thirty two 16-bit registers are provided which configure and control the operation of the CVXI-1149.1 card. The registers are located in the VXIbus A16 address space within a 40 hex address block that is selected by the 8 bit logical address DIP switch. Chapter 4 provides a complete description of the VXIbus A16 registers.

ADDRESS OFFSET	REGISTER	READ/WRITE
\$00	VXI ID Register	Read
\$02	VXI Device Type	Read
\$04	VXI Status/Control	Read/Write
\$06	Trigger-In Select Register	*Read/Write
\$08	Digital I/O Port #1	Read/Write
\$0A	Digital I/O Port #2	Read/Write
\$0C	Configuration Register #1	Read/Write
\$0E	Configuration Register #2	Read/Write
\$10-\$3E	SN74ACT8990 Registers	Read/Write

* Note: Read-back register is implemented using two JTAG compatible 74BCT8244 devices.

VME/VXIbus Interface

The CVXI-1149.1 is an A16/D16 VME/VXIbus compatible slave module. The card is designed to accept A16 mode address modifiers 29 hex and 2D hex. The card occupies 64 bytes (32 words) of VXI/VME address space. The card address within the A16 address space is set by an 8 bit DIP switch that selects one of 255 address blocks from \$C000 to \$FF80 in \$40 (64 byte) increments.

All the on-board registers are 16 bits wide and are accessed via D16 data transfer cycles on the VME/VXIbus.

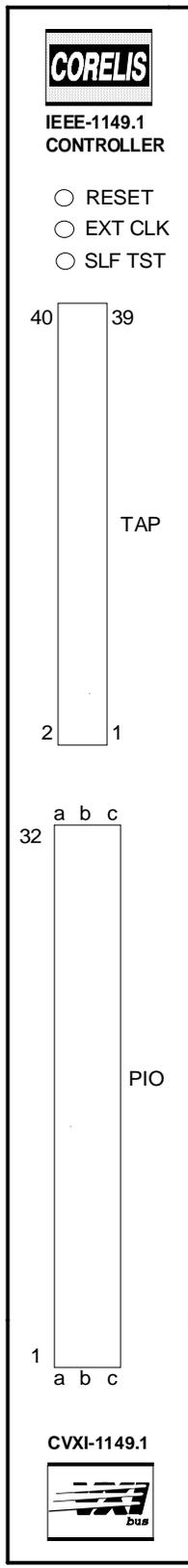


Figure 1-4 CVXI-1149.1 Front Panel

CVXI-1149.1 Specifications

VME/VXibus Interface

Configurable Logical Addresses	1 through 254 (default = 32)
I/O Width	D16 only
I/O Space Size	64 bytes (offsets \$00 - \$3F)
Configurable IRQs	IRQ1 through IRQ7 (default = No IRQ connected)

IEEE-1149.1

Number of TAP Controllers	6
Maximum TCK frequency	12.5 MHz
Maximum scanning data length	2 ³² bits

Parallel Ports

Output Voltage Compatibility	LS-TTL
Output Current	24 ma (low), -2.6 ma (high)
Input Voltage Compatibility	LS-TTL
Input Current	One LS-TTL load and 220/330Ω termination to VCC/GND

Physical

Board Outline Dimensions (PCB)	C Size: 13.4" x 9.2" x 1.2" B Size: 6.3" x 9.2" x 0.8"
I/O Connectors	1 JTAG Interface Connector 40-pin IDC [3M P/N 3432-5202 or equivalent] 1 Parallel I/O Connector 96-pin DIN [Harting P/N 09-03-196-6921 or equivalent]

Power Requirements

5 volts	2A maximum
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Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non condensing

Storage Environment

Temperature	-40°C to 85°C
Relative Humidity	0% to 100%, non condensing

About this Chapter

This chapter contains essential information regarding required hardware and software to operate the CVXI-1149.1 Boundary Scan Controller Card. These requirements are described in the following sections:

- Introduction
- VXIbus Operation
- System Software

Introduction

To implement a VXIbus system, an appropriate VXIbus mainframe (or card cage) with which to enclose, support inter-module triggering over the VXIbus, and provide necessary power is required. The CVXI-1149.1 is designed to operate correctly when installed within any standard VXIbus card cage systems that support C or B size modules.

To direct operation of installed VXIbus instruments, a host computer is required. This host can either be located externally, or be embedded within the VXIbus enclosure system. However, which of the two configurations is more advantageous depends on your system requirements. For example, an external host may become necessary when use of a specific set of software tools are mandated. On the other hand, if it is possible to use an embedded VXIbus-based computer, the simplification of the physical design, improvement in throughput, and the potential for cost savings are important advantages to consider.

VXIbus Operation

The CVXI-1149.1 is designed principally for VXIbus operation which provides for its highest level of capability. When operated in that environment, a wide range of system configurations are supported that can accommodate a broad class of applications, particularly those requiring many instruments. The B size card, however, can be operated in any VMEbus compatible chassis. Although the VXIbus specification imparts considerable architectural flexibility, for the purposes of this manual, only 'standard' approaches to operating the CVXI-1149.1 will be discussed. More elaborate configurations (e.g. multiple host computers, etc.) are beyond the scope of this manual.

The basic elements required for an operational VXIbus system employing an external host computer are:

- 1 - VXIbus Card Cage
- 2 - VXIbus Slot 0 Controller/Resource Manager with GPIB Interface
- 3 - CVXI-1149.1 Module
- 4 - Other VXIbus Instrument Modules
- 5 - Host Computer with GPIB
- 6 - GPIB Cable
- 7 - Host GPIB Software Drivers

Note: (A number of companies are offering alternative interfaces to the GPIB. This includes the 16-bit parallel MXI Interface, Ethernet, and others. For simplicity, only GPIB will be referenced in this manual.)

Alternatively, the basic elements required for an operational VXIbus system employing an embedded host computer are:

- 1- VXIbus Compatible Embedded Host Computer
(may or may not have built-in Slot 0 features)
- 2 - VXIbus Card Cage
- 3 - CVXI-1149.1 Module
- 4 - VXIbus Slot 0 Controller/Resource Manager
- 5 - Other VXIbus Instrument Modules
- 6 - Host-based VXIbus Instrument Software Drivers

Card Cages

The CVXI-1149.1 requires a card cage designed to VXIbus Specification Rev 1.2 or higher supporting C-size modules. The B size version of the CVXI-1149.1 card will operate in any B-size VXIbus or VMEbus compatible chassis. You can install as many CVXI-1149.1 modules into a single card cage as is allowed electrically and physically. Power and available slots are often the main limiting factors. The card requires a single +5V power supply with 2 amps maximum capability.

The card cage must provide forced-air cooling sufficient to maintain proper CVXI-1149.1 component temperatures. It is suggested that the internal card cage air temperature not exceed 60 degrees Centigrade with a minimum air velocity of 0.1 ft/sec at both sides of the module.

Slot 0 Controller/Resource Manager

To operate the CVXI-1149.1 in a VXIbus configuration, at least one Slot 0 Controller/Resource Manager or its equivalent function must be present in the VXIbus chassis. This function, as described in the VXIbus specification, manages hardware resources tied to the VXIbus and generally also provides a GPIB interface to the host computer. Although they must all provide a minimum subset of functional features as described in the VXIbus specification, these controllers are available in many forms, each having specific key features. For example, some slot 0 controllers include the equivalent of an entire host computer (see below) thereby making possible a stand-alone VXIbus based instrument system with embedded controller in a single card cage.

As to the type of Slot 0 Controller/Resource Manager you choose for your system depends on the goals and available hardware. The VXIbus standard is quite flexible with regard to topology and therefore many paths may be possible for a given requirement. However, it is generally best to employ the least complex approach where possible.

Host Computer

The CVXI-1149.1 requires a host computer to direct its operation. This host can either be embedded into the VXIbus card cage or located externally and linked to the VXIbus card cage via GPIB. Any computer having a GPIB port can potentially serve as an external host. Likewise, virtually any VXIbus-based computer operating as a bus commander can function as a host. If the host computer is embedded inside the VXIbus card cage, communication with the CVXI-1149.1 is register based. Alternatively, if an embedded host has GPIB, it can link to the VXIbus slot 0 controller installed in the same or other VXIbus card cage(s) over GPIB. This may be desirable in situations calling for a consistent set of instrument drivers conversant with a single communication protocol such as GPIB. Therefore when using an embedded controller to conserve space, the former requirement is satisfied by employing its GPIB channel as the primary instrument control linkage, into and out of the VXIbus environment. Figure 2-1 illustrates these basic configurations.

GPIB Host Interface

If the host is to reside external to the VXIbus system, a GPIB interface is required. Most computers that have GPIB interfaces can be used to control the CVXI-1149.1 via VXIbus communication protocols. To correctly operate the remote VXIbus system, appropriate GPIB commands must be issued. This is generally accomplished using software drivers that are either supplied by the VXIbus Slot 0 manufacturer or user written.

System Software

In VXIbus external host computer configurations, host software drivers will be required to issue appropriate GPIB commands, VXIbus Slot 0 Controller commands, and VXIbus Instrument commands. Drivers for the GPIB and Slot 0 Controller/Resource Manager are usually supplied by the manufacturers of the GPIB interface and Slot 0 Controller respectively. "C" source drivers are provided on a diskette with each CVXI-1149.1 Module.

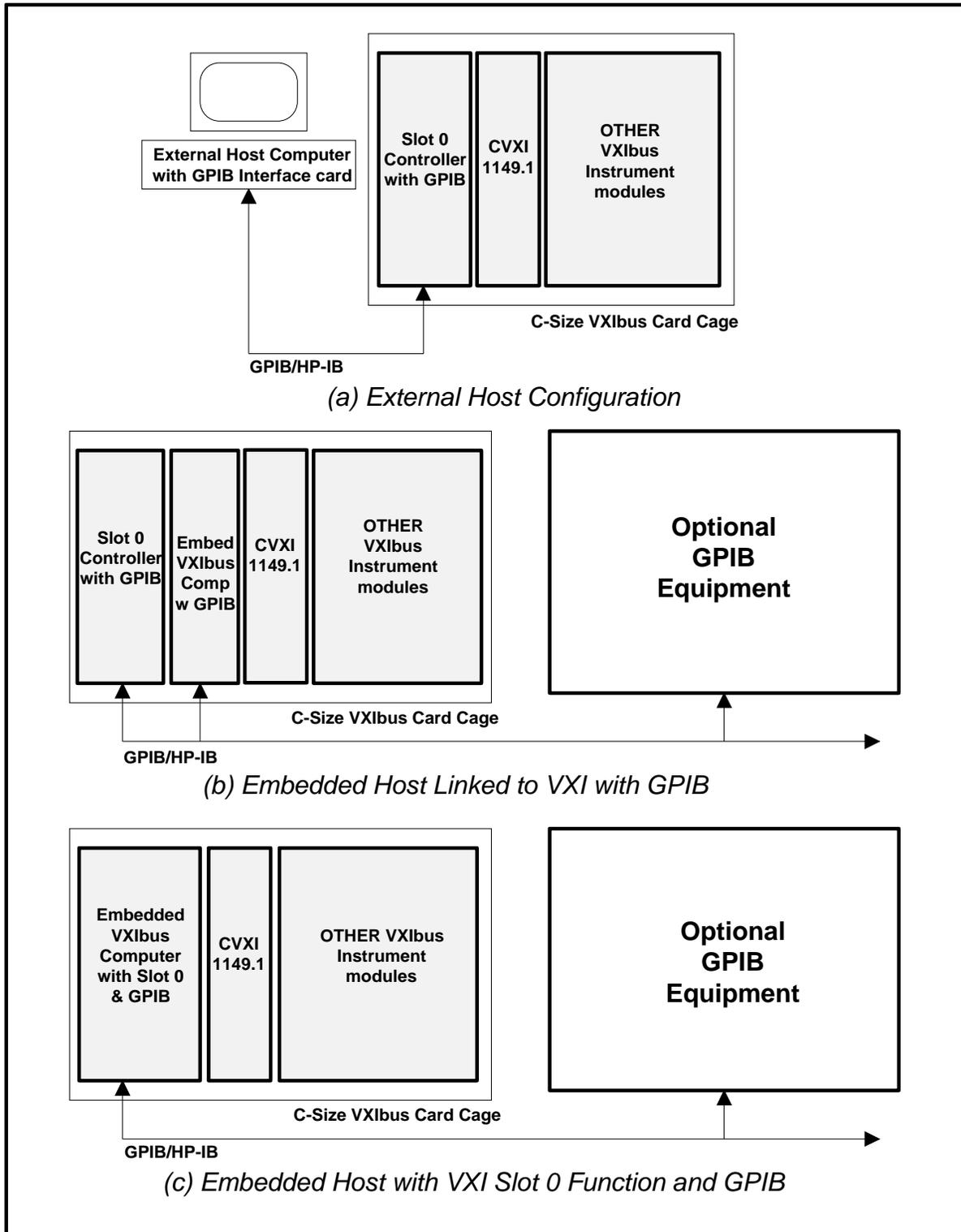


Figure 2-1 Example Host/VXI Linkage Configurations

About this Chapter

This chapter contains important handling and VXIbus installation/configuration information for the CVXI-1149.1 Boundary Scan Controller Card. Configuring the CVXI-1149.1 to operate in your VXIbus system involves the setting of hardware switches which may have to be performed prior to installation. This information is comprised of the following sections:

- Unpacking and Inspection
- Hardware Configuration

Unpacking and Inspection

To avoid possible damage and voiding of product warranty, it is imperative that the following handling procedures be observed:

Unpacking

This product is packaged to protect it from possible causes of damage either by physical means or by electrostatic discharge (ESD). It is important that an appropriate location be used to perform unpacking. Such an area should be free of the possibility for ESD and present no risk of physical damage.

IMPORTANT: *If there is any sign of significant damage to the original shipping carton, report it immediately to CORELIS and the shipping company.*

Once the original shipping carton has been opened and the individual items have been removed, place them together for inspection. The CVXI-1149.1 hardware is packaged in anti-static protective material and should be carefully removed to avoid destruction of this packing. Retain this along with the other packing materials for possible future transport.

Inspection

The CVXI-1149.1 module should be free of any signs of physical damage. If this is not the case, consult immediately with CORELIS or its authorized sales representative for advisory information.

Hardware Configuration

The VXIbus standard provides for modules of many purposes and manufacturers to reside in a single VXIbus card cage. To operate together, all such modules in a VXIbus system must be properly hardware configured. Therefore, before installing your CVXI-1149.1 module into the VXIbus system card cage and applying power, it may have to be configured differently than the factory setting. Once configured, these modules are then able to be managed by means of software commands via standard VXIbus communication protocols.

***NOTE:** If you have already established how you are to configure the Logical Address of the CVXI-1149.1, you can skip to the **Logical Address Selector** sub-section.*

VXIbus System Planning

Due to the diversity of features found in VXIbus system elements, it is important to understand the detailed requirements and capabilities of the specific modules you plan to install in your system and how they are to interact. For example, not all Slot 0 Controller modules (or their equivalents) are created equal. That is due to the fact that suppliers often differentiate their products by providing useful proprietary high level features that assist VXIbus system implementation. As a result, such features can have great influence on the topological approach selected during VXIbus system design.

An important step in the design process is the planning of the VXIbus system structure by establishing module hierarchy such as commander-servant relationships. This is best done by charting out the full list of instruments and required control modules based on available features and your system requirements. Figure 3-1 provides an example chart that can be used for this purpose. However, details of how to best configure your system are beyond the scope of this manual.

Although the VXIbus specification contains fundamental information in this regard, more practical knowledge can be obtained from user's manuals of VXIbus modules, particularly those of VXIbus controllers. The reason for this is that controller products embody many of the primary system features that most influence configuration possibilities.

Configuration

The CVXI-1149.1 module possesses a Logical Address DIP switch with which to manually determine specific address configurations from 0 to 255. A setting of 0 is reserved for slot 0 controller modules, and the value 255 is reserved to signal that the VXIbus resource manager is to perform dynamic logical address configuration on the instrument. The CVXI-1149.1 does not support dynamic logical address configuration.

The instrument must be set to an address between 1 and 254, so the module is, in VXI terminology, configured *statically*.

NOTE: *No two modules should have the same Logical Address in any group of VXIbus modules being controlled by the same slot 0/resource manager*

Logical Address Selector

Once your VXIbus system hierarchical structure has been determined, the next step is to configure the CVXI-1149.1 logical address to the chosen value. The factory default is set to 32. If you wish to change this, the proper position for each of the 8 switches yielding the desired value must be determined.

NOTE: *As shown in Figure 3-2 the Logical Address DIP Switch, accessed through the module cover, forms its value based on the sum of the decimal values of the switches in the OPEN (1) position. Examples of this are shown in this figure.*

VXIbus Chassis Slot

The CVXI-1149.1 can be installed into any available VXIbus backplane slot except slot 0.

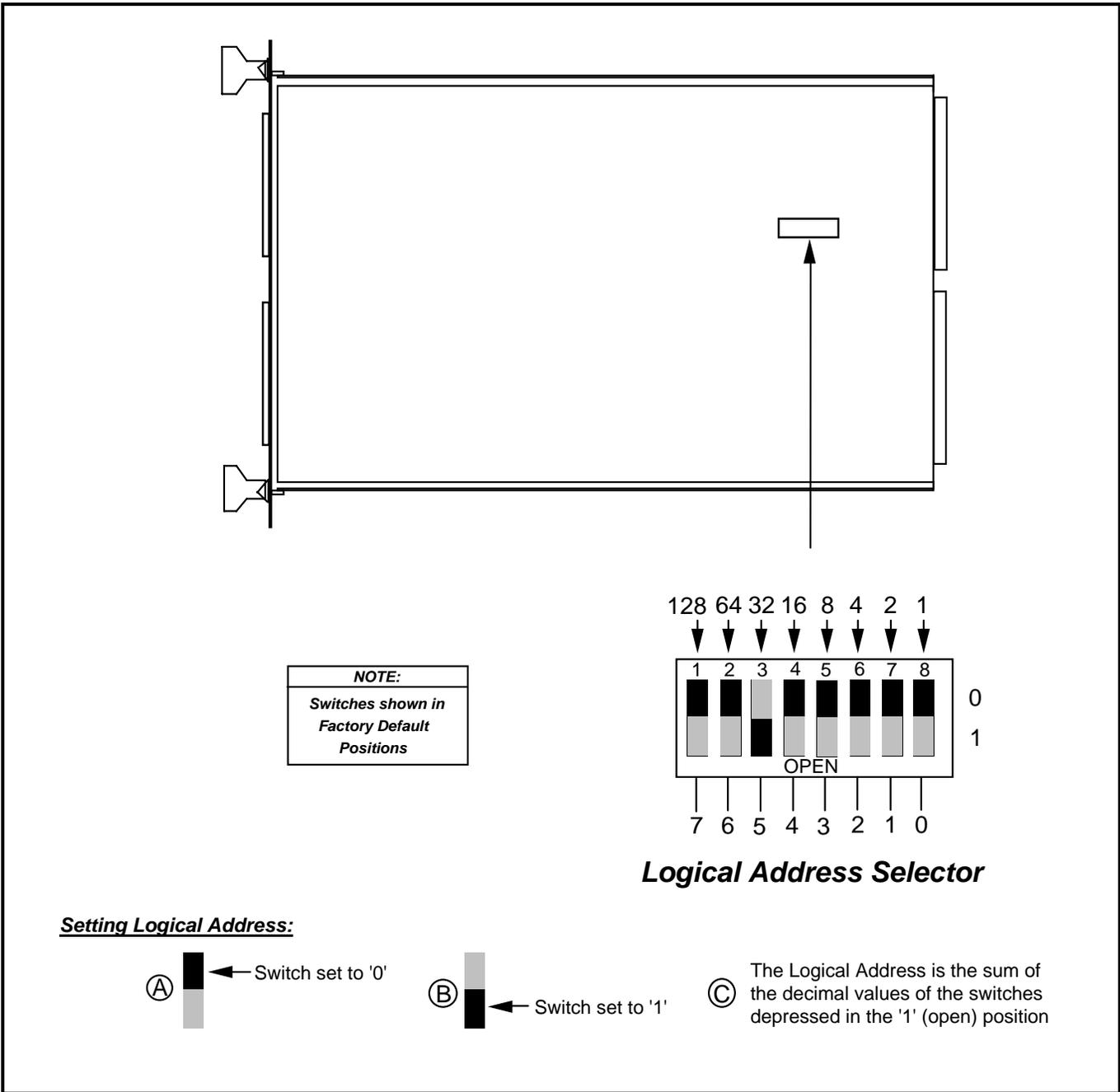


Figure 3-2 Logical Address Selector DIP Switch

About this Chapter

This chapter contains information regarding the description of the CVXI-1149.1 hardware. This information is contained in the following sections:

- Front Panel LED's
- Front Panel Connectors
- A16 Registers
- ID Register
- Device Type Register
- VXI Status Register
- Trigger-in Select Register
- TSR Read-Back Register
- Digital Output Register #1
- Digital Input Register #1
- Digital Output Register #2
- Digital Input Register #2
- Configuration Register #1
- Configuration Register #2
- TBC Chip Registers

Front Panel LEDs

The three CVXI-1149.1 card front panel LED's are described in table 4-1. The LED's are directly controlled by the appropriate bits in Configuration Register #1:

LED	COLOR	DESCRIPTION
RESET	Amber	Illuminates when the TRGRST* bit (D6) of Control Register #1 is asserted (low).
EXT CLK	Green	Illuminates when the CLKSEL1 bit (D12) of Control Register #1 is set to "1" (high).
SLF TST	Green	Illuminates when the TRGOFF* bit (D5) of Control Register #1 is asserted (low).

Table 4-1 Front Panel LED Description

Front Panel Connectors

JTAG Connector

The JTAG interface connector (labeled TAP) is a 40-pin 3M type connector that includes all the signals for the six serial boundary scan access ports. This connector is located on the upper portion of the front panel of the card. The pinout of the TAP connector is shown in table 4-2.

PIN	SIGNAL NAME	I/O	DESCRIPTION
1	TRST*	Out	Target reset command signal
3	TDO	Out	Test Data Output
5	TDI0	In	Test Data Input - Channel 0
7	TMS0	Out	Test Mode Select - Channel 0
9	TCK	Out	Test Serial Clock
11	T_OFF*	In	"Target power off" indicator (active low)
13	SENSE*	In	"Target cable connected" sense line
15	TCKI	In	External clock signal from the target
17	TDI1	In	Test Data Input - Channel 1
19	TMS1	Out	Test Mode Select - Channel 1
21	EVENT0	In	SN74ACT8990 EVENT0 signal
23	EVENT1	In	SN74ACT8990 EVENT1 signal
25	EVENT2	In	SN74ACT8990 EVENT2 signal
27	EVENT3	In	SN74ACT8990 EVENT3 signal
29	TEST_TDI	In	TDI of the on-board test circuit (BCT8244's)
31	TEST_TDO	Out	TDO of the on-board test circuit (BCT8244's)
33	TEST_TMS	In	TMS of the on-board test circuit (BCT8244's)
35	TEST_TCK	In	TCK of the on-board test circuit (BCT8244's)
37	TMS2	Out	Test Mode Select - Channel 2
38	TMS4	Out	Test Mode Select - Channel 4
39	TMS3	Out	Test Mode Select - Channel 3
40	TMS5	Out	Test Mode Select - Channel 5

All other pins of the connector (2,4,6,8...,36) are connected to ground (GND).

Table 4-2 JTAG Interface Pinout

PIO Connector

The PIO connector is a standard Eurocard 96-pin male DIN connector. This connector can be used to interface non-JTAG circuitry to the CVXI-1149.1 parallel I/O ports in order to support testing of target systems that incorporate both JTAG and non-JTAG circuitry. There are 32 parallel inputs and 32 parallel outputs that connect to rows A and C of the 3 row 96-pin DIN connector. Row B is connected to ground. The pin-out of the PIO connector is shown in tables 4-3 and 4-4.

DIGITAL I/O	BIT	PIO CONNECTOR PIN
Digital Input Register #1	0 (LSB)	A1
Digital Input Register #1	1	A2
Digital Input Register #1	2	A3
Digital Input Register #1	3	A4
Digital Input Register #1	4	A5
Digital Input Register #1	5	A6
Digital Input Register #1	6	A7
Digital Input Register #1	7	A8
Digital Input Register #1	8	A9
Digital Input Register #1	9	A10
Digital Input Register #1	10	A11
Digital Input Register #1	11	A12
Digital Input Register #1	12	A13
Digital Input Register #1	13	A14
Digital Input Register #1	14	A15
Digital Input Register #1	15 (MSB)	A16
Digital Output Register #1	0 (LSB)	A17
Digital Output Register #1	1	A18
Digital Output Register #1	2	A19
Digital Output Register #1	3	A20
Digital Output Register #1	4	A21
Digital Output Register #1	5	A22
Digital Output Register #1	6	A23
Digital Output Register #1	7	A24
Digital Output Register #1	8	A25
Digital Output Register #1	9	A26
Digital Output Register #1	10	A27
Digital Output Register #1	11	A28
Digital Output Register #1	12	A29
Digital Output Register #1	13	A30
Digital Output Register #1	14	A31
Digital Output Register #1	15 (MSB)	A32

Table 4-3 PIO Connector Row A Pinout

DIGITAL I/O	BIT	PIO CONNECTOR PIN
Digital Input Register #2	0 (LSB)	C1
Digital Input Register #2	1	C2
Digital Input Register #2	2	C3
Digital Input Register #2	3	C4
Digital Input Register #2	4	C5
Digital Input Register #2	5	C6
Digital Input Register #2	6	C7
Digital Input Register #2	7	C8
Digital Input Register #2	8	C9
Digital Input Register #2	9	C10
Digital Input Register #2	10	C11
Digital Input Register #2	11	C12
Digital Input Register #2	12	C13
Digital Input Register #2	13	C14
Digital Input Register #2	14	C15
Digital Input Register #2	15 (MSB)	C16
Digital Output Register #2	0 (LSB)	C17
Digital Output Register #2	1	C18
Digital Output Register #2	2	C19
Digital Output Register #2	3	C20
Digital Output Register #2	4	C21
Digital Output Register #2	5	C22
Digital Output Register #2	6	C23
Digital Output Register #2	7	C24
Digital Output Register #2	8	C25
Digital Output Register #2	9	C26
Digital Output Register #2	10	C27
Digital Output Register #2	11	C28
Digital Output Register #2	12	C29
Digital Output Register #2	13	C30
Digital Output Register #2	14	C31
Digital Output Register #2	15 (MSB)	C32

Table 4-4 PIO Connector Row C Pinout

A16 Registers

Table 4-5 lists all the A16 registers on the CVXI-1149.1 module. The registers are shown sorted by their address offset from the base address of the module.

Address Offset	A16 Register	Accessibility
\$00	VXI ID Register (always reads \$FF00)	Read
\$02	VXI Device Type Register (always reads \$047D)	Read
\$04	VXI Status Register	Read
\$06	VXI Trigger-In Select Register (TSR)	Write
\$06	TSR Read-Back Register (Two 74BCT8244 JTAG IC's)	Read
\$08	Digital Output Register #1	Write
\$08	Digital Input Register #1	Read
\$0A	Digital Output Register #2	Write
\$0A	Digital Input Register #2	Read
\$0C	Configuration Register #1	Read/Write
\$0E	Configuration Register #2	Read/Write
\$10	TBC Control0 Register	Read/Write
\$12	TBC Control1 Register	Read/Write
\$14	TBC Control2 Register	Read/Write
\$16	TBC Control3 Register	Read/Write
\$18	TBC Control4 Register	Read/Write
\$1A	TBC Control5 Register	Read/Write
\$1C	TBC Control6 Register	Read/Write
\$1E	TBC Control7 Register	Read/Write
\$20	TBC Control8 Register	Read/Write
\$22	TBC Control9 Register	Read/Write
\$24	TBC Minor Command Register	Read/Write
\$26	TBC Major Command Register	Read/Write
\$28	TBC Counter1 Update0 Register	Read/Write
\$2A	TBC Counter1 Update1 Register	Read/Write
\$2C	TBC Counter2 Update0 Register	Read/Write
\$2E	TBC Counter2 Update1 Register	Read/Write
\$30	TBC Status0 Register	Read
\$32	TBC Status1 Register	Read
\$34	TBC Status2 Register	Read
\$36	TBC Status3 Register	Read
\$38	TBC Capture0 Register	Read
\$3A	TBC Capture1 Register	Read
\$3C	TBC Read Buffer Register	Read
\$3E	TBC Write Buffer Register	Write

Table 4-5 CVXI-1149.1 A16 Registers

Absolute A16 Addressing

Some software requires the user to specify the absolute A16 address of a register to be accessed. The base address of the CVXI-1149.1 can be calculated by using the following formula:

$$\text{\$C000} + (\text{Logical_Address} * \text{\$40})$$

or (decimal)

$$49,152 + (\text{Logical_Address} * 64)$$

The address $\text{\$C000}$ is defined by VXIbus as the beginning of A16 space which is dedicated to each module installed in a system. Each logical address in a VXIbus system is dedicated 64 bytes of the upper 16Kb of A16 space.

The factory set logical address is 32 which yields a base address of:

$$\text{\$C000} + (32 * \text{\$40})$$

$$\text{\$C000} + \text{\$0800} = \text{\$C800}$$

or (decimal)

$$49,152 + (32 * 64)$$

$$49,152 + 2048 = \mathbf{51,200}$$

To access registers on the card, the offset of the register is added to the base address of the card to form a complete A16 address. For example, configuration register #1 has an offset of $\text{\$0C}$. Adding this offset to the base address of $\text{\$C800}$ (assuming the default logical address 32) yields an A16 address of $\text{\$C80C}$.

ID Register

The CVXI-1149.1 ID Register indicates the classification, addressing mode, and the manufacturer of the device.

Address	15 - 14	13 - 12	11 - 0
Base + \$00	Device Class	Address Mode	Manufacturer ID

Device Classification: Bits 15 and 14 classify a device as one of the following:

- 00** memory device
- 10** extended device
- 10** message-based device
- 11** register based device

The CVXI-1149.1 module is a register based device.

Addressing Mode: Bits 13 and 12 indicate the addressing mode used by the device:

- 00** A16/A24 address mode
- 01** A16/A32 address mode
- 10** RESERVED
- 11** A16 address mode only

The CVXI-1149.1 module uses the A16 address mode only.

Manufacturer ID: Bits 11 through 0 identify the manufacturer of the device. The Corelis ID number is 3840 which corresponds to bits 11-0 being set to \$0F00.

Given the device classification, addressing space, and manufacturer of the CVXI-1149.1 module, reading the ID register will always return the value \$FF00.

Device Type Register

The Device Type register contains a model code which identifies the device.

Address	15 - 12	11-0
Base + \$02	Required Memory	Model Code

Required Memory: Since the CVXI-1149.1 is an A16 only device, this field will always be zero.

Model Code: The model code which identifies the CVXI-1149.1 module is \$047D (1149 decimal).

VXI Status Register

The VXI status register contains status bits for various functions of the CVXI-1149.1 card. The register content is described in the following table:

Address	15	14	13	12	11	10	9	8 - 4	3	2	1	0
Base + \$04	0	MODID*	0	RDY*	INT*	SENSE*	TOFF	0	1	1	0	0

MODID* This bit indicates the status of the VXIbus MODID signal. The slot 0 controller uses this active low bit to select cards in the VXIbus chassis.

RDY* This active low bit reflects the state of the SN74ACT8990 (TBC) RDY signal. When asserted, it indicates that the TBC is ready for additional commands and/or data.

INT* This active low bit reflects the state of the SN74ACT8990 (TBC) INT signal. When asserted, it indicates that the TBC is sending an interrupt to the host.

SENSE* This bit, when low, indicates that the SENSE signal on the JTAG interface connector is connected to GND. This signal can be used by the software to sense that an external cable is connected to the card JTAG connector.

TOFF This bit, when high, indicates that the target power is off at the JTAG interface connector.

Trigger-In Select Register

The VXI Trigger-in Select Register (TSR) selects which of the eight TTLTRG* trigger lines will be used as an input to each of the four EVENT inputs of the SN74ACT8990 TBC chip.

Address	15-12	11-8	7-4	3-0
Base + \$06	Event 3 Select	Event 2 Select	Event 1 Select	Event 0 Select

The TSR register content is described in the following tables:

REGISTER BITS D3-D0				SELECT FUNCTION
1	0	0	0	VXibus TTLTRG0* is input to TBC EVENT0
1	0	0	1	VXibus TTLTRG1* is input to TBC EVENT0
1	0	1	0	VXibus TTLTRG2* is input to TBC EVENT0
1	0	1	1	VXibus TTLTRG3* is input to TBC EVENT0
1	1	0	0	VXibus TTLTRG4* is input to TBC EVENT0
1	1	0	1	VXibus TTLTRG5* is input to TBC EVENT0
1	1	1	0	VXibus TTLTRG6* is input to TBC EVENT0
1	1	1	1	VXibus TTLTRG7* is input to TBC EVENT0
0	X	X	X	No signal is connected to the TBC EVENT0

REGISTER BITS D7-D4				SELECT FUNCTION
1	0	0	0	VXibus TTLTRG0* is input to TBC EVENT1
1	0	0	1	VXibus TTLTRG1* is input to TBC EVENT1
1	0	1	0	VXibus TTLTRG2* is input to TBC EVENT1
1	0	1	1	VXibus TTLTRG3* is input to TBC EVENT1
1	1	0	0	VXibus TTLTRG4* is input to TBC EVENT1
1	1	0	1	VXibus TTLTRG5* is input to TBC EVENT1
1	1	1	0	VXibus TTLTRG6* is input to TBC EVENT1
1	1	1	1	VXibus TTLTRG7* is input to TBC EVENT1
0	X	X	X	No signal is connected to the TBC EVENT1

REGISTER BITS D11-D8				SELECT FUNCTION
1	0	0	0	VXIbus TTLTRG0* is input to TBC EVENT2
1	0	0	1	VXIbus TTLTRG1* is input to TBC EVENT2
1	0	1	0	VXIbus TTLTRG2* is input to TBC EVENT2
1	0	1	1	VXIbus TTLTRG3* is input to TBC EVENT2
1	1	0	0	VXIbus TTLTRG4* is input to TBC EVENT2
1	1	0	1	VXIbus TTLTRG5* is input to TBC EVENT2
1	1	1	0	VXIbus TTLTRG6* is input to TBC EVENT2
1	1	1	1	VXIbus TTLTRG7* is input to TBC EVENT2
0	X	X	X	No signal is connected to the TBC EVENT2

REGISTER BITS D15-D12				SELECT FUNCTION
1	0	0	0	VXIbus TTLTRG0* is input to TBC EVENT3
1	0	0	1	VXIbus TTLTRG1* is input to TBC EVENT3
1	0	1	0	VXIbus TTLTRG2* is input to TBC EVENT3
1	0	1	1	VXIbus TTLTRG3* is input to TBC EVENT3
1	1	0	0	VXIbus TTLTRG4* is input to TBC EVENT3
1	1	0	1	VXIbus TTLTRG5* is input to TBC EVENT3
1	1	1	0	VXIbus TTLTRG6* is input to TBC EVENT3
1	1	1	1	VXIbus TTLTRG7* is input to TBC EVENT3
0	X	X	X	No signal is connected to the TBC EVENT3

This register bits will be all 0's upon power-up reset.

Trigger-In Select Read-Back Register

The Trigger-In Select Read-Back register is a 16-bit wide buffer that enables the user to read back data from the Trigger-in Select Register (TSR). The TSR Read-Back register is implemented using two 74BCT8244 buffer IC's that are also IEEE-1149.1 (JTAG) compatible.

When the target JTAG interface is turned off (see Configuration Register #1 description), the two 74BCT8244 devices are automatically connected to the first of the six on-board JTAG channels (channel 0). The operation of the JTAG Test Access Port (TAP) can now be verified using this "simple" on-board JTAG circuitry. First, the software writes arbitrary data to the TSR, then it reads the TSR Read-Back register and verifies that the appropriate data is received. The data can be read from the TSR Read-Back register either directly, or via the JTAG interface.

Address	15 - 0
Base + \$06	16 Bit Word

Digital Output Register #1

The digital output register #1 is a parallel output register that provides up to sixteen general purpose TTL outputs. This register is a write only register and can be used to send discrete control signals to the JTAG target to support non-JTAG compatible circuitry on the target system.

Address	15 - 0
Base + \$08	16 Bit Word

Digital Input Register #1

The digital input register #1 is a parallel input register that provides up to sixteen general purpose TTL inputs. This register is a read only register and can be used to input discrete control signals from the target system.

Address	15 - 0
Base + \$08	16 Bit Word

Digital Output Register #2

The digital output register #2 is a parallel output register that provides sixteen additional general purpose TTL outputs that, together with digital output register #1 total 32 TTL outputs. This register is a write only register and can be used to send discrete control signals to the JTAG target to support non-JTAG compatible circuitry on the target system.

Address	15 - 0
Base + \$0A	16 Bit Word

Digital Input Register #2

The digital input register #2 is a parallel input register that provides additional sixteen general purpose TTL inputs. Together with digital input register #1, a total of 32 TTL inputs are available to the user. This register is a read only register and can be used to input discrete control signals from the target system.

Address	15 - 0
Base + \$0A	16 Bit Word

Configuration Register #1

Configuration register #1 is a read/write register that determines certain modes of operation for the JTAG interface logic. These register bits will be all 0's upon power-up reset. The register is described in the following table:

Address	15	14	13	12	11 - 8
Base + \$0C	Unused	FREE_RUN	Unused	CLKSEL1	BYTEN

Address	7	6	5	4	3 - 0
Base + \$0C	STEP*	TRGRST*	TRGOFF*	CLKSEL0	DIV

DIV3-0 These 4 bits determine the divider used to generate the JTAG interface TCK serial shift clock as per the following table:

DIV 3	DIV 2	DIV 1	DIV 0	DIVIDER
0	0	0	0	Divide by 2
0	0	0	1	Divide by 4
0	0	1	0	Divide by 6
0	0	1	1	Divide by 8
0	1	0	0	Divide by 10
0	1	0	1	Divide by 12
0	1	1	0	Divide by 14
0	1	1	1	Divide by 16
1	0	0	0	Divide by 18
1	0	0	1	Divide by 20
1	0	1	0	Divide by 22
1	0	1	1	Divide by 24
1	1	0	0	Divide by 26
1	1	0	1	Divide by 28
1	1	1	0	Divide by 30
1	1	1	1	Divide by 32

CLKSEL 1-0 Select the clock source for the JTAG interface. Once the clock source is selected, it will be divided by the prescaler pointed by the DIV3-0 bits and then used by the JTAG circuitry. The CLKSEL bits function as shown in the following table:

CLKSEL1	CLKSEL0	CLOCK SOURCE
0	0	Internal clock - 25 MHz
0	1	Internal clock - 781 KHz
1	0	VXibus TTLTRG signal
1	1	External clock (JTAG Connector)

TRGOFF* This active low signal causes the JTAG interface to the target system to go tri-state and electrically disconnect itself from the target.

When the TRGOFF* signal is low, the two on-board JTAG compatible 74BCT8244 devices are connected in series with the channel 0 signals of the SN74ACT8990 TBC chip. This enable self-test and diagnostics software to fully test the functionality of the JTAG interface prior to attaching it to the target system.

TRGRST* This active low signal directly drives the on-board SN74ACT8990 TBC chip reset input pin. It also drives the TRST* signal on the front panel JTAG connector.

The TRST* signal is defined in the IEEE-1149.1 specification as an optional Test Access Port signal. It can be used to reset the target JTAG interface and circuitry.

STEP* An active low single-step control signal that enables the software to directly drive the JTAG clock signal and be able to single step the interface logic under software control. When asserted, the TCK signal is driven directly by the DIV0 bit of this register.

BYTEN These four bits control the enabling of the 32 parallel outputs. The description of each bit is given in the following table:

Bit	Mnemonic	Description
8	BYTEN1	An active high byte-enable signal for the discrete output register. When this bit is asserted, the least significant eight bits of Output Register #1 are enabled.
9	BYTEN2	An active high byte-enable signal for the discrete output register. When this bit is asserted, the most significant eight bits of Output Register #1 are enabled.
10	BYTEN3	An active high byte-enable signal for the discrete output register. When this bit is asserted, the least significant eight bits of Output Register #2 are enabled.
11	BYTEN4	An active high byte-enable signal for the discrete output register. When this bit is asserted, the most significant eight bits of Output Register #2 are enabled.

FREE_RUN This bit, when set, indicates that the TCK output (pin 9) on the TAP Connector will free-run. Otherwise, the TCK output will be controlled by the 74ACT8990 (TCKO).

Configuration Register #2

Configuration register #2 is a read/write register that selects VXIbus interrupts and triggers to/from the SN74ACT8990 (TBC) chip. This register will be set to 0 upon power-up reset.

Address	15 - 11	10 - 8	7 - 4	3 - 0
Base + \$0E	not used	EXTCLK	TTLTRG* Select	VXI INTR* Select

The register is described in the following table:

REGISTER BITS D3-D0				SELECT FUNCTION
1	0	0	0	No VXIbus interrupt is active
1	0	0	1	TBC INT-is connected to VXIbus IRQ1*
1	0	1	0	TBC INT-is connected to VXIbus IRQ2*
1	0	1	1	TBC INT-is connected to VXIbus IRQ3*
1	1	0	0	TBC INT-is connected to VXIbus IRQ4*
1	1	0	1	TBC INT-is connected to VXIbus IRQ5*
1	1	1	0	TBC INT-is connected to VXIbus IRQ6*
1	1	1	1	TBC INT-is connected to VXIbus IRQ7*
0	X	X	X	No signal is connected to the VXIbus interrupt lines

Bits D3 - D0 select which VXIbus interrupt line the SN74ACT8990 interrupt will be connected to.

REGISTER BITS D7-D4				SELECT FUNCTION
1	0	0	0	TBC INT is connected to VXIbus TTLTRG0*
1	0	0	1	TBC INT is connected to VXIbus TTLTRG1*
1	0	1	0	TBC INT is connected to VXIbus TTLTRG2*
1	0	1	1	TBC INT is connected to VXIbus TTLTRG3*
1	1	0	0	TBC INT is connected to VXIbus TTLTRG4*
1	1	0	1	TBC INT is connected to VXIbus TTLTRG5*
1	1	1	0	TBC INT is connected to VXIbus TTLTRG6*
1	1	1	1	TBC INT is connected to VXIbus TTLTRG7*
0	X	X	X	No signal is connected to the VXIbus trigger lines

Bits D7 - D4 select which VXIbus TTL trigger line the SN74ACT8990 interrupt will be connected to.

REGISTER BITS D10-D8			SELECT FUNCTION
0	0	0	TTLTRG0* is connected to JTAG clock mux
0	0	1	TTLTRG1* is connected to JTAG clock mux
0	1	0	TTLTRG2* is connected to JTAG clock mux
0	1	1	TTLTRG3* is connected to JTAG clock mux
1	0	0	TTLTRG4* is connected to JTAG clock mux
1	0	1	TTLTRG5* is connected to JTAG clock mux
1	1	0	TTLTRG6* is connected to JTAG clock mux
1	1	1	TTLTRG7* is connected to JTAG clock mux

Bits D10-D8 select a VXibus TTL trigger line as an external source for the JTAG clock. Note that the JTAG clock is selected from a 4 input mux by programming the CLKSEL 1,0 bits in Configuration Control Register #1.

Bits D15-D11 are unused and can be utilized by the software for testing/diagnostics.

SN74ACT8990 Registers

A detailed description of the SN74ACT8990 Test Bus Controller (TBC) chip registers is provided in Appendix B.

About this Chapter

This chapter describes the "C" source coded self-test software and drivers that are provided with each CVXI-1149.1 module. This is comprised of the following sections:

- Introduction
- Hardware Configuration
- scan_ir() routine
- scan_dr() routine
- circulate_dr() routine
- hard_reset() routine
- wait_jtag_state() routine
- soft_reset() routine
- check_ready() routine
- wait_for_ready() routine
- write_tbc() routine
- read_tbc() routine
- write_buf() routine
- read_buf() routine
- Selftest Software Listings

Introduction

The sample "C" code diskette provided with the CVXI-1149.1 card is intended to serve two functions. First, this code is the actual C language source code for the executable selftest program included on the disk. Second, this code provides functions which will be useful either directly or as example code to a programmer writing software to operate the CVXI-1149.1. Three different versions of the software are supplied to support various hosts. All source code was compiled with the Borland C compiler.

The functions provided in the source code can be classified in two categories:

- Scanning
- Utility/Low-level access

The Scanning functions provide a higher level access to the operation of the SN74ACT8990 IC. These functions are:

scan_ir(unsigned short *output, unsigned short length, unsigned short *input)

This function scans an arbitrary length bit stream into the TAP controller instruction register. This function takes three parameters. The *output* parameter is an address to an array of 16-bit values to be scanned out the JTAG instruction path. The *length* parameter specifies the length of the bit stream (pointed to by *output*). The *input* parameter specifies the address of 16-bit values where the data scanned in is to be stored.

scan_dr(unsigned short *output, unsigned short length, unsigned short *input)

This function scans an arbitrary length bit stream through the TAP controller data path. This function takes three parameters. The *output* parameter is an address to an array of 16-bit values to be scanned out the JTAG data path. The *length* parameter specifies the length of the bit stream (pointed to by *output*). The *input* parameter specifies the address of 16-bit values where the data scanned in is to be stored.

circulate_dr(unsigned short length, unsigned short *data)

This function circulates an arbitrary length bit stream through the TAP controller data path. This is accomplished by initially shifting dummy data through the TAP data path to get valid data out, and then reshifting the valid data back into the path. This allows a data path to be inspected without modifying its contents. This function takes two parameters. The *length* parameter specifies the length of the bit stream to be circulated. The *data* parameter specifies the address of 16-bit values where the data scanned in is to be stored.

The utility/low-level functions are as follows:

hard_reset(unsigned short target, unsigned short divider)

This function causes a hardware reset of the SN74ACT8990 by pulsing its *TRST input. This also causes the *TRST line of the JTAG targets to be pulsed. The result of hardware reset on the chip should be reviewed in the SN74ACT8990 data sheet. This function takes two parameters. The *target* parameter can have two possible values, 0 or 1. A value of 0 specifies the ACT8990 is to be connected to the external JTAG targets, and a value of 1 specifies the ACT8990 is to be connected to the internal JTAG 8244 devices, and the external JTAG target interface is tri-stated. The *divider* parameter specifies a value from 0 to 15 which selects one of the TCK clock dividers (see the *control* register).

wait_jtag_state(short state)

This function waits until the JTAG bus has transitioned to the specified state. The *state* parameter specifies one of the JTAG bus states as defined at the start of the test program.

soft_reset(void)

This function causes a software only reset of the SN74ACT8990. The result of soft reset on the chip should be reviewed in the SN74ACT8990 data sheet. This function takes no parameters.

check_ready(void)

The check ready function is used by the low level read and write functions associated with the SN74ACT8990 to verify that the chip is ready for additional accesses. It returns a 1 if the SN74ACT8990 is ready to be accessed, and 0 otherwise. This function takes no parameters.

wait_for_ready(void)

This function does not return until the SN74ACT8990 is ready to be accessed. This is implemented by continually polling the *status* register until a value of 0 is read in the RDY* bit position. This function takes no parameters.

write_tbc(unsigned short register_offset, unsigned short data)

This function writes a data value to one of the SN74ACT8990 registers. The function first verifies that *register_offset* is a valid offset. When the SN74ACT8990 is ready to be accessed (by calling *wait_for_ready()*) the data is written to the specified register. No checking is done to see if the register is a read only register. This function takes two parameters. The *register_offset* parameter specifies which register on the SN74ACT8990 to write, and the *data* parameter specifies the data to be written.

read_tbc(unsigned short register_offset, unsigned short *data)

This function reads a data value from one of the SN74ACT8990 registers. The function first verifies that *register_offset* is a valid offset. When the SN74ACT8990 is ready to be accessed (by calling *wait_for_ready()*) the data is read from the specified register and stored at the specified location. No checking is done to see if the register is a write only register. This function takes two parameters. The *register_offset* parameter specifies which register on the SN74ACT8990 to read, and the *data* parameter specifies the address where the read data is to be stored.

write_buf(unsigned short data)

This function writes a data value to the SN74ACT8990 output shift register. It polls the SN74ACT8990 STATUS2 register until the *write_OK* flag indicates data may be written to the shift register buffer, at which time the specified data is written out. This function takes one parameter *data* which is the data to be stored in the output shift register.

read_buf(unsigned short *data)

This function reads a data value from the SN74ACT8990 input shift register. It polls the SN74ACT8990 STATUS2 register until the *read_OK* flag indicates data is available to be read, at which time the input shift register buffer is read. This function takes one parameter *data* which specifies the address where the read data is to be stored.

Selftest Software Source Code

C language source code is provided for the selftest software. Several different versions of the software are supplied for various interfaces. Check the CVXI-1149.1 selftest software and driver disk for available source code. Currently, the supported interfaces are as follows:

1. RadiSys EPC-2/2e 80386 or EPC-7 80486 Embedded PC.
2. National Instruments MXI interface.
3. National Instruments LabWindows.
4. Hewlett-Packard's E1405A slot-0 controller using an HP IEEE-488 controller card installed in a PC.

APPENDIX A

SELFTEST SOFTWARE SOURCE CODE LISTINGS

Refer to the CVXI-1149.1 Self-Test Software and Driver Disk.

APPENDIX B
SN74ACT8990 APPLICATION NOTE

The following pages contain the SN74ACT8990 application note.