

NetUSB II

NetUSB II
High-Speed JTAG Controller

User's Manual

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Table of Contents

Chapter 1: Product Overview	1
Introduction.....	1
What is IEEE Standard 1149.1?.....	1
Product Versions	2
Features of the NetUSB II	2
Absolute Maximum Ratings.....	4
Recommended Operating Conditions.....	4
Specifications.....	4
Chapter 2: NetUSB II Installation & Use	7
Package Contents.....	7
Microsoft Windows Software Installation	7
Linux Software Installation	8
Hardware Installation.....	8
Chapter 3: Use with ScanExpress Tools.....	11
Overview.....	11
Hardware Setup.....	11
Chapter 4: Third Party Application Interface	21
Using the NetUSB II with ScanExpress Runner API.....	21
Using the NetUSB II with the Scan Function Library.....	25
Chapter 5: Recommended Target Connectors.....	27
10-pin TAP Connector	27
16-pin Flash Programming TAP Connector	29
20-pin Flash Programming & Power Test TAP Connector.....	32
Direct I2C Direct Programming Connector.....	35
Direct SPI Programming Connector	36
Chapter 6: Self-Test Application.....	37
Overview.....	37
Loopback Cables.....	37
Running the Test	37
Chapter 7: Firmware Update Utility	39
Overview.....	39

Updating the Firmware.....	39
Appendix A: GNU Licenses.....	41
GNU GENERAL PUBLIC LICENSE.....	41
GNU LESSER GENERAL PUBLIC LICENSE.....	46

Table of Figures

Figure 1-1. NetUSB II 4-TAP (left) and NetUSB II 8-TAP (right) JTAG Controllers.....	1
Figure 1-2. JTAG Controller Test Access Port (TAP)	1
Figure 1-3. Net USB II 4-TAP front panel (left) and rear panel (right).....	2
Figure 2-1 Example Entry in Windows Device Manager	7
Figure 2-2. NetUSB II Network Configuration Tool.....	9
Figure 3-1. NetUSB II Controller Configuration	12
Figure 3-2. NetUSB II Advanced Configuration.....	15
Figure 3-3. Pinout Configuration Dialog.....	17
Figure 3-4. NetUSB II Parallel Outputs.....	18
Figure 5-1. Standard 10-pin TAP Connector (top view).....	27
Figure 5-2. 10-pin TAP Connector Schematic.....	28
Figure 5-3. Boundary-scan Flash Programming 16-pin TAP Connector (top view).....	29
Figure 5-4. 16-pin Flash Programming TAP Connector Schematics.....	31
Figure 5-5. Boundary-scan Flash Programming with Power Test Points 20-pin TAP Connector (top view) ..	32
Figure 5-6. 20-pin Flash Programming with Power Test Points Connector Schematics.....	34
Figure 5-7. Direct I2C Programming Connector Schematics.....	35
Figure 5-8. SPI Direct Programming Connector Schematics.....	36
Figure 6-1. NetUSB II Self-Test Results.....	38
Figure 7-1. NetUSB II Firmware Update Utility	39
Figure 7-2. Firmware Update Confirmation Dialog.....	40
Figure 7-3. Firmware Update Success Dialog.....	40

Table of Tables

Table 1-1. NetUSB II Model Descriptions.....	2
Table 1-2. Power & Status Indicator States.....	3
Table 1-3. Absolute Maximum Ratings.....	4
Table 1-4. Recommended Operating Conditions.....	4
Table 3-1. TAPs Voltage options.....	12
Table 3-2. Programmable TCK Frequencies.....	13
Table 3-3. TAPs Configuration options.....	13
Table 3-4. SPI/I2C TAPs options.....	14
Table 3-5. TAPs Off State options.....	14
Table 3-6. Delay Compensation options.....	15
Table 3-7. TCK Mode options.....	16
Table 3-8. TAP Configuration - Threshold options.....	16
Table 3-9. TAP Configuration - Pinouts options.....	17
Table 3-10. Standard Pinouts.....	17
Table 3-11. NetUSB II Parallel Outputs Mapping.....	18
Table 4-1. NetUSB II Controller Parameters.....	21
Table 4-2. Pinout Values.....	25
Table 5-1. 10-pin TAP Signal Description and Termination.....	28
Table 5-2. Standard 10-Pin TAP Connector.....	28
Table 5-3. Flash Programming TAP 16-Pin Connector.....	29
Table 5-4. 16-pin TAP Signal Description and Termination.....	30
Table 5-5. Flash Programming TAP 20-pin Connector.....	32
Table 5-6. 20-pin TAP Signal Description and Termination.....	33
Table 5-7. I2C Signal Description and Recommended Termination.....	35
Table 5-8. SPI Signal Description and Recommended Termination.....	36
Table 6-1. Self-Test Loopback Cable Connections.....	37

Chapter 1: Product Overview

Introduction

The NetUSB II 4-TAP and 8-TAP High-Speed JTAG Controllers are members of the Corelis ScanExpress™ family of scan-based test, analysis, and diagnostic tools. The NetUSB II interfaces between a PC equipped with a USB2.0 or Ethernet port and any IEEE Standard 1149.1 compatible target. The NetUSB II is designed to control the operation of an IEEE Standard 1149.1 boundary-scan (JTAG) test access port (TAP) by generating the proper signals under software control to interface with the target device. It supports scan operations at continuous JTAG clock (TCK) speeds of up to 100 MHz.



Figure 1-1. NetUSB II 4-TAP (left) and NetUSB II 8-TAP (right) JTAG Controllers.

The NetUSB II facilitates software-controlled boundary-scan operations defined by IEEE Standard 1149.1. It provides command access to the target's Test Access Port (TAP), accessing device internal registers and on-chip debugger, verifying PCB interconnects, performing functional testing, and debug without manual probing. The JTAG interface also provides access to internal device functions that are not accessible via external probing, enabling fault isolation within the device itself. The JTAG interface also enables programming target flash and CPLD devices, as well as data download and upload to and from the target memory devices.

What is IEEE Standard 1149.1?

The IEEE-1149.1 Test Access Port Interface (TAP) shown in Figure 1-2 consists of four required signals:

- Test Data In (TDI)
- Test Data Out (TDO)
- Test Mode Select (TMS)
- Test Clock (TCK)

A fifth signal is defined as optional:

- Test Reset (TRST*)

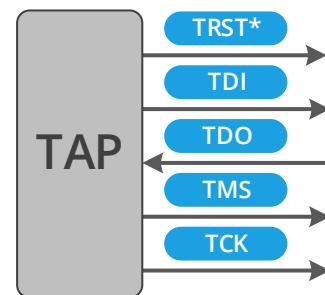


Figure 1-2. JTAG Controller Test Access Port (TAP)

Product Versions

The NetUSB II is available in a 4-TAP or 8-TAP configuration, as described in Table 1-1 below. The 4-TAP front and rear panels are pictured in Figure 1-3 below.

Table 1-1. NetUSB II Model Descriptions

Part Number	Product Name	Description
10504	NetUSB II 4-TAP	NetUSB II high-speed JTAG controller with 4 TAP connectors
10508	NetUSB II 8-TAP	NetUSB II high-speed JTAG controller with 8 TAP connectors



Figure 1-3. Net USB II 4-TAP front panel (left) and rear panel (right).

Features of the NetUSB II

The Corelis NetUSB II is a sophisticated test controller that can access devices, boards or systems compliant with IEEE Standard 1149.1.

TAP Interface

Configurable JTAG, SPI, I²C, & GPIO Signals

Each TAP includes 8 configurable signal pins. These pins can be configured to provide JTAG, serial peripheral interface (SPI), Inter-Integrated Circuit (I²C), or general-purpose input/output (GPIO) capabilities. Pin order can be customized, and each TAP can be configured with different signal types.

In addition to general functions, the GPIO signals may be designated as flash ready/busy handshake input or as external write pulse signal to significantly improve in-system-programming (ISP) speeds.

Adjustable Voltage

The software-programmable voltage level of the TAP interfaces and discrete I/O can be set to any voltage between 1.00 V and 3.30 V in increments of 0.05 V.

Programmable Clock

The NetUSB II's programmable TCK output to the IEEE Standard 1149.1 compatible target system can be generated with a wide range of frequencies using the programmable clock generator.

Pin Protection

The NetUSB II features 5 V tolerant signals, board-level ESD protection, and voltage detection circuitry to prevent the drivers from being damaged if the outputs are inadvertently shorted to power or ground.

Power Supply Short Detection

Each TAP on the NetUSB II can detect a target power supply short to ground for up to 2 voltages. This allows the NetUSB II to discover potentially damaging conditions before the target system is powered up.

Serial TAP Chaining

The NetUSB II TAPs can be programmed to daisy-chain sub-sets of the TAP ports into single chains.

Concurrent TAP Operation

During gang (concurrent) TAP operations, all targets can be scanned simultaneously. While scanning, each TAP returns scanned information that is compared against expected patterns for verification and possible mismatch error detection. An unexpected pattern on any individual TAP will be logged but need not necessarily stop the scan session for the others. This method can be used for rapid flash memory content validation on a large set of targets concurrently.

Delay Compensation

The NetUSB II delay compensation feature allows higher clock frequencies on TCK to be used by adjusting when data on TDO coming back from the target is sampled by the hardware in half clock increments.

USB 2.0 Port Interface

The NetUSB II USB interface complies with the version 2.0 standard with backward compatibility to version 1.1 (excluding low speed). Speed adjustment is automatic per the standard. The hot-plug feature of this standard is fully supported such that attachment is easily made to a running PC, which will automatically sense its presence. For optimal performance, a host PC with a USB 2.0 port is strongly recommended.

Ethernet Port Interface

The NetUSB II Ethernet interface supports 10/100/1000Base-T with automatic speed switching and is IEEE 802.3, 802.3u and 802.3ab compatible.

Power Connector & Power Switch

The NetUSB II connects to a 12 V DC Power Supply (included). The power switch is used to turn the NetUSB II on when connected to power.

Power & Status Indicator LED

The front panel includes a green LED labeled **Power** to indicate unit status. When powered on, the NetUSB II undergoes a boot process when powered on that typically lasts approximately 30 seconds. After the boot process is completed, the LED remains on steadily to indicate that the unit is ready for use. Table 1-2 below describes the LED status modes.

Table 1-2. Power & Status Indicator States

Status	Description
Off	The NetUSB II is powered off.
Blinking green	The NetUSB II is currently booting. The boot process can take up to 30 seconds.
Solid green	The NetUSB II is ready for use.

Active Cooling

The NetUSB II includes an automatically controlled internal fan to control the unit temperature. Ventilation holes on the left and right panels of the NetUSB II allow for air flow.

Note: The ventilation holes must not be obscured to allow proper airflow. Inadequate ventilation could result in damage to the NetUSB II.

Absolute Maximum Ratings

Table 1-3. Absolute Maximum Ratings

Symbol	Description	Limit Min	Limit Max	Units
V _I	DC Input Voltage	-0.30	+5.25	V
I _O	DC Output Current	-40	+40	mA
T _{STG}	Ambient Storage Temperature	-65	150	°C
T _A	Ambient Operating Temperature	-40	85	°C

Recommended Operating Conditions

Table 1-4. Recommended Operating Conditions

Symbol	Description	Limit Min	Limit Max	Units
V _{IH}	High Level Input Voltage	V _{ADJ} * 0.5	5.00	V
V _{IL}	Low Level Input Voltage	0.0	V _{ADJ} * 0.5	V
R _O	DC Output Resistance	45	55	Ω
I _O	DC Output Current	-25	+25	mA
T _{STG}	Ambient Storage Temperature	-40	85	°C
T _A	Ambient Operating Temperature	0	45	°C

Specifications

Host Computer System Requirements

Interface	Available USB 2.0-compatible or 10/100/1000Base-T Ethernet port
Operating System	Microsoft Windows 7 Microsoft Windows 8/8.1 Microsoft Windows 10 Linux (Scan Function Library only)

Host Interface Compliance

USB	2.0 High Speed
Ethernet	10/100/1000Base-T (IEEE 802.3, 802.3u or 802.3ab)

I/O Cable Connectors

USB Connector	Standard USB type B socket
Ethernet Connector	Standard RJ-45 socket
TAP Connectors	Four (4-TAP) or Eight (8-TAP) 2 × 10 pin shrouded headers 0.1 inch × 0.1 inch spacing with long ejectors (3M 3428-6302 or equivalent)

JTAG Interface

TCK frequency range	0.1 MHz to 100 MHz
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SPI Interface

SCK frequency 0.1 MHz to 50 MHz

I²C Interface

SCL frequency 100 kHz

Power Requirements

12 V \pm 5% 4 A maximum

Physical Dimensions

NetUSB II 4-TAP 5.71 inches \times 6.24 inches \times 2.14 inches

NetUSB II 8-TAP 5.71 inches \times 6.24 inches \times 3.09 inches

Chapter 2: NetUSB II Installation & Use

Package Contents

The standard NetUSB II product package contains the following components:

- One NetUSB II High-Speed JTAG Controller Hardware (4-TAP or 8-TAP)
- One 12 V power adapter
- Four (4-TAP) or eight (8-TAP) 30 cm 20-pin shielded TAP cables
- One 2-meter USB Cable (A-to-B type)
- One 2-meter Ethernet Cable (RJ45 compatible)

Ensure all materials listed are present and free from visible damage or defects before proceeding. If anything appears to be missing or damaged, please contact Corelis at support@corelis.com or the number listed on the front cover.

It is suggested that you preserve the original packing material in the event the product must be shipped back to Corelis for service.

Microsoft Windows Software Installation

Refer to the instructions included with your software package for software installation instructions. The NetUSB II is supported under ScanExpress Tools version 8.6 or later and Corelis Scan Function Library (SFL) version 2.20 or later.

The NetUSB II uses the Remote Network Driver Interface Specification (RNDIS) included with current versions of Microsoft Windows for communication over USB. When plugged into a USB port, the controller will be listed in the device manager as a **Remote NDIS Compatible Device** as shown in Figure 2-1 below.

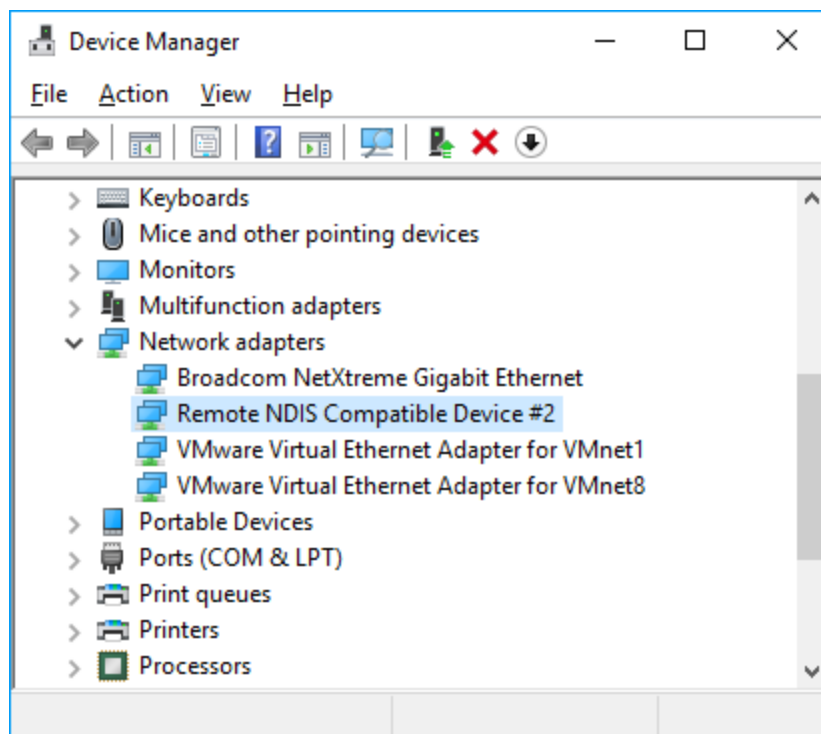


Figure 2-1 Example Entry in Windows Device Manager

Note: A device driver is not required when using the NetUSB II controller in Microsoft Windows 7, 8, or 10. Unsupported device drivers are available for use with legacy versions of Microsoft Windows.

Linux Software Installation

Limited support for Linux environments is supported using the Scan Function Library (SFL). Consult the **NetUSB II SFL User's Manual** for more details on using the NetUSB II SFL.

Note: The NetUSB II requires a Linux kernel with TCP/IP and RNDIS support. The NetUSB II was verified to be compatible with Ubuntu 14.04 LTS.

Hardware Installation

Using the NetUSB II Over USB

To install the NetUSB II on PC using a USB port:

1. Connect the NetUSB II to an available USB port on your PC using the supplied USB cable.
2. Connect the power adapter to the NetUSB II power connected labeled **12V DC** and plug the power adapter into an electrical outlet.
3. Toggle the switch labeled **Power** to the **ON** position.

The front panel Power LED will blink during the power up sequence and remain on when the NetUSB II is ready for operation.

Using the NetUSB II Over Ethernet

To use the NetUSB II over network connection, network parameters must first be configured using a USB connection. A configuration utility is included with the ScanExpress Tools or Scan Function Library software. To configure the network parameters:

1. Follow the steps described in the section titled **Using the NetUSB II Over USB** above.
2. Wait 30 seconds for the power up sequence to complete.
3. Execute "**C:\Program Files (x86)\Common Files\Coreelis Shared\12.0\NetUSB-II_Config.exe**".

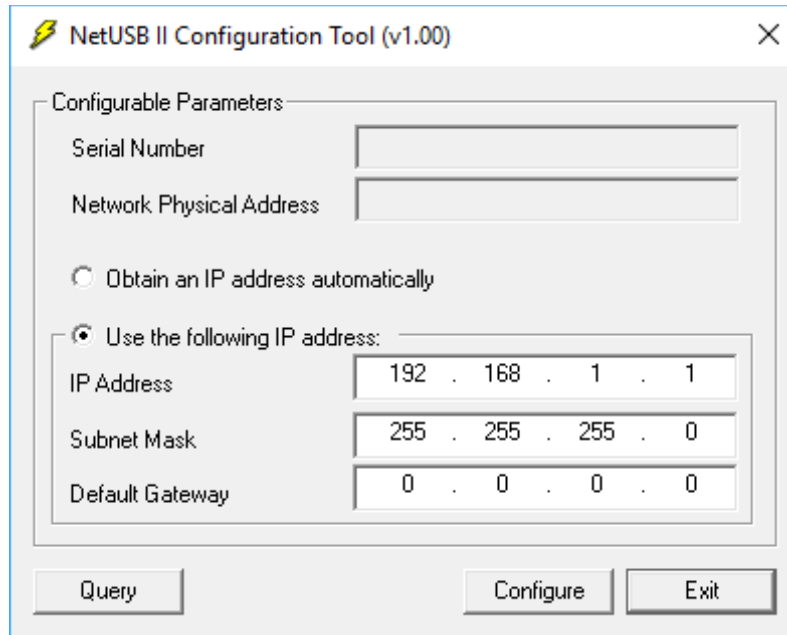


Figure 2-2. NetUSB II Network Configuration Tool

4. Enter the appropriate network parameters. For example:
 - IP Address: default value = 192.168.1.1
 - Subnet Mask: default value = 255.255.255.0
 - Default Gateway: default value = 0.0.0.0
5. Click the **Configure** button.
6. Cycle power by toggling the **Power** switch to the **OFF** position and then back to the ON position. The new settings will take effect when the NetUSB II boots.
7. Click the **Query** button to read the current configuration.

Note: The NetUSB II uses port 6471 when communicating over the network. If the NetUSB II is behind a firewall, port 6471 must be opened.

Chapter 3: Use with ScanExpress Tools

Overview

The NetUSB II controller is compatible with all ScanExpress applications. The following steps are provided for ScanExpress Runner; configuration of the NetUSB II controller in the other ScanExpress applications is done in a similar fashion. Some controller configuration options are available as test step options in ScanExpress Runner. Refer to the ScanExpress Runner User's Manual for details.

Hardware Setup

You must configure the NetUSB II controller inside the ScanExpress application before the application can use it. This chapter uses ScanExpress Runner as an example to illustrate the configuration process.

NetUSB II Controller Selection

1. Make sure that the NetUSB II controller is plugged in to network port and is properly configured with desired network settings as detailed in the section titled “**Microsoft Windows Software Installation**”.
2. Wait 30 seconds before starting any ScanExpress applications if you just powered up the controller.
3. launch the **ScanExpress Runner** application.
4. Click the **Setup** menu item and then select the **Controller** entry to display the **Controller Configuration** dialog.
5. Select the **NetUSB II** controller from the icons on the left. Adjust the settings to the desired values. Note that the controller uses port 6471 when communicating over the network; if the controller is behind a firewall, make sure to open port 6471.
6. After making your selections, click **Apply** to test and save the settings. When the program saves the settings successfully, it displays the controller in the **Current Controller** box. If ScanExpress Runner cannot find the controller, it will display an error dialog.

NetUSB II Controller Configuration

The main parameters of the NetUSB II controller are configured in the **Controller Configuration** dialog shown in Figure 3-1 below.

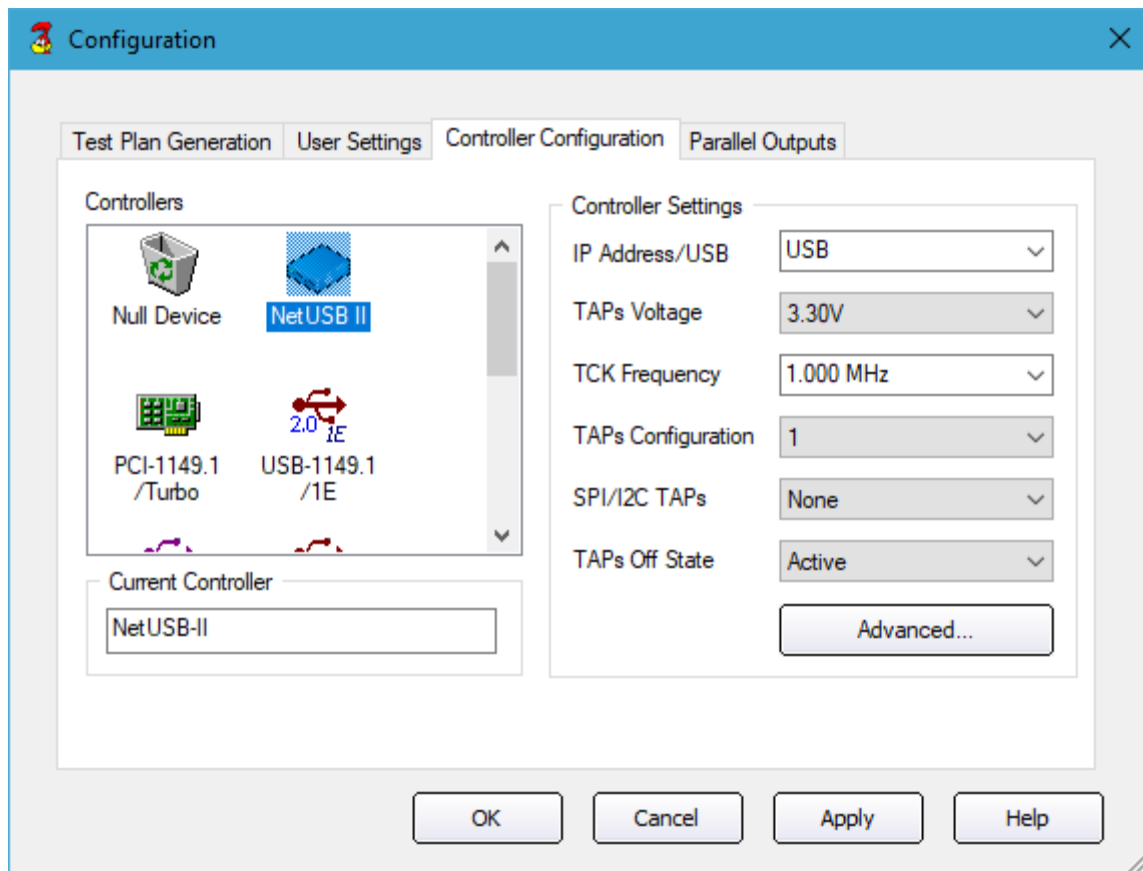


Figure 3-1. NetUSB II Controller Configuration

IP Address/USB

Select “USB” when using the USB interface or enter a network IP address when using the Ethernet interface.

TAPs Voltage

The “TAPs Voltage” setting configures all TAP signals and GPIO to a fixed voltage between 1.00 V and 3.30 V. For multiple TAP voltages, select “Advanced” and select the voltage for each TAP in the **NetUSB II Advanced Configuration** dialog.

Table 3-1. TAPs Voltage options

TAPs Voltage Selection	Description
1.00V to 3.30V	All TAPs configured with the selected voltage.
Advanced	Individual TAPs configured with the voltage selected in the NetUSB II Advanced Configuration dialog.

TCK Frequency

The “TCK Frequency” setting sets the clock rate for TCK (JTAG) and SCK (SPI). Valid selections are described in Table 3-2 below.

Table 3-2. Programmable TCK Frequencies

TCK Range (MHz)	Frequency Resolution (MHz)
0.1 to 0.9	0.1
1.0 to 100.0	1.0

Note: The clock (SCL) for I2C Direct Programming is always fixed at 100 kHz.

TAPs Configuration

The “TAPs Configuration” setting selects the TAP(s) to be used. Valid selections are described in Table 3-3 below.

Table 3-3. TAPs Configuration options

TAPs Configuration	Description
1	TAP 1 (default)
2	TAP 2
3	TAP 3
4	TAP 4
5	TAP 5
6	TAP 6
7	TAP 7
8	TAP 8
1+2	Chain TAP 1 – TAP 2
1+2+3	Chain TAP 1 – TAP 3
1+2+3+4	Chain TAP 1 – TAP 4
1+...+5	Chain TAP 1 – TAP 5
1+...+6	Chain TAP 1 – TAP 6
1+...+7	Chain TAP 1 – TAP 7
1+...+8	Chain TAP 1 – TAP 8

SPI/I2C TAPs

The “SPI/I2C TAPs” setting configures a TAP for I2C or SPI Direct Programming. Valid selections are shown in Table 3-4 below.

Table 3-4. SPI/I2C TAPs options

SPI/I2C TAPs	Description
None	None (default)
1	TAP 1 used for I2C/SPI
2	TAP 2 used for I2C/SPI
3	TAP 3 used for I2C/SPI
4	TAP 4 used for I2C/SPI
5	TAP 5 used for I2C/SPI
6	TAP 6 used for I2C/SPI
7	TAP 7 used for I2C/SPI
8	TAP 8 used for I2C/SPI

TAPs Off State

When set to “Active,” the boundary-scan controller will drive TAP signals between tests and when set to “Tri-State,” the TAP signals will be tri-stated (not driven) between tests. Valid selections are shown in Table 3-5 below.

Table 3-5. TAPs Off State options

TAPs Off State	Description
Active	ScanExpress Runner will not tri-state the JTAG interface upon completion of a test plan execution.
Tri-State	ScanExpress Runner will tri-state the JTAG interface upon completion of a test plan execution. Enables TAP signal protection.

A TAP signal protection feature is enabled when the off state is set to “Tri-State.” Under these conditions, ScanExpress Runner will test the TAP output signals (TMS, TDI, and TCK) to determine if they are shorted to power. If ScanExpress Runner detects that any of the TAP output signals are shorted to power, it will stop the execution of the test to prevent damage to the hardware.

NetUSB II Advanced Configuration

Click **Advanced** under **Controller Settings** to bring up the **NetUSB II Advanced Configuration** dialog shown in Figure 3-2 below.

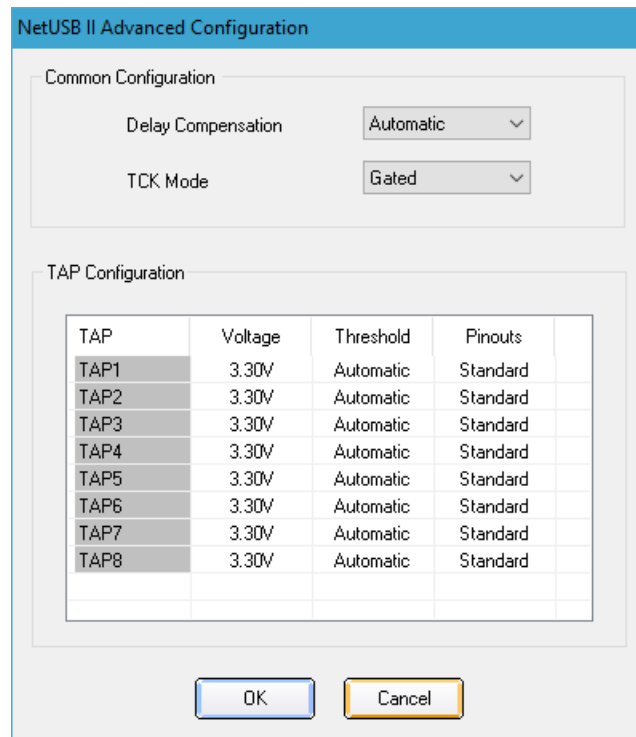


Figure 3-2. NetUSB II Advanced Configuration

Delay Compensation

The NetUSB II's delay compensation feature allows higher clock frequencies on TCK to be used by adjusting when data on TDO coming back from the target is sampled by the hardware in half clock increments. Valid selections are shown in Table 3-6 below.

Table 3-6. Delay Compensation options

Delay Compensation	Description
Automatic	Delay compensation will be automatically selected based on the selected TCK frequency. This is the default option.
No Delay	TDO will be sampled with no delay.
0.5 Clock	TDO will be sampled after 0.5 clock periods delay.
1 Clock	TDO will be sampled after 1 clock period delay.
1.5 Clocks	TDO will be sampled after 1.5 clock periods delay.
2 Clocks	TDO will be sampled after 2 clock periods delay.
2.5 Clocks	TDO will be sampled after 2.5 clock periods delay.
3 Clocks	TDO will be sampled after 3 clock periods delay.
3.5 Clocks	TDO will be sampled after 3.5 clock periods delay.

TCK Mode

The “TCK Mode” setting configures the behavior of TCK in-between scan operations and the JTAG bus is parked in one of the four stable states (Test-Logic-Reset, Run-Test/Idle, Pause-DR, or Pause-IR). Valid selections are shown in Table 3-7 below.

Table 3-7. TCK Mode options

TCK Mode	Description
Gated (default)	TCK will be held low between scan operations. This is the default option.
Continuous	The state machine will be moved to one of the four stable states (Test-Logic-Reset, Run-Test/Idle, Pause-DR, or Pause-IR) and TCK will continuously toggle between scan operations.

Note: Continuous TCK mode does not guarantee that TCK will always remain active. The NetUSB II may stop the clock under certain conditions.

TAP Configuration – Voltage

This set of options configures separate voltages for each TAP when the **TAPs Voltage** setting in the main controller dialog is set to “Advanced”. Valid selections include “0.100V” to “3.30V.”

TAP Configuration – Threshold

This set of options configures separate input signal threshold voltages for each TAP. When set to “Automatic,” a threshold level equal to one half of the selected **Voltage** setting. Valid selections are shown in Table 3-8 below.

Table 3-8. TAP Configuration - Threshold options

Threshold	Description
Automatic	The input threshold will be one half of the selected Voltage setting.
0.50V to 2.00V	The input threshold will be equal to the selected value.

TAP Configuration – Pinouts

This set of options configures the pinout for each TAP. Valid selections are shown in Table 3-9 below.

Table 3-9. TAP Configuration - Pinouts options

Pinouts	Description
Standard	The Corelis standard pinouts will be used for JTAG and SPI/I2C TAPs. These pinouts are shown in Table 3-10.
Custom	A custom pinout will be used for JTAG and SPI/I2C TAPs. When this option is selected, the Pinout Configuration dialog shown in Figure 3-3 will be displayed and allow a pin to be selected for each JTAG or SPI/I2C signal.

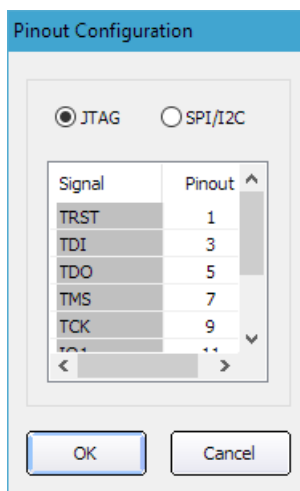


Figure 3-3. Pinout Configuration Dialog

The default pinouts for JTAG, SPI, and I2C are shown in Table 3-10 below.

Table 3-10. Standard Pinouts

Pin	JTAG	I2C	SPI
1	TRST*	SDA	SCK
2	GND	GND	GND
3	TDI	SCL	MOSI
4	GND	GND	GND
5	TDO		MISO
6	GND	GND	GND
7	TMS		CS0*
8	GND	GND	GND
9	TCK		CS1*
10	GND	GND	GND
11	Write_Strobe* / GPIO1		CS2*
12	GND	GND	GND
13	GPIO2		CS3*
14	GND	GND	GND
15	Ready_Busy* / GPIO3		CS4*
16	GND	GND	GND
17	VCC1	VCC1	VCC1
18	NC	NC	NC
19	VCC2	VCC2	VCC2
20	NC	NC	NC

Parallel Outputs

The **Parallel Outputs** tab configures the GPIO before and after a test has run as well as upon termination of ScanExpress Runner.

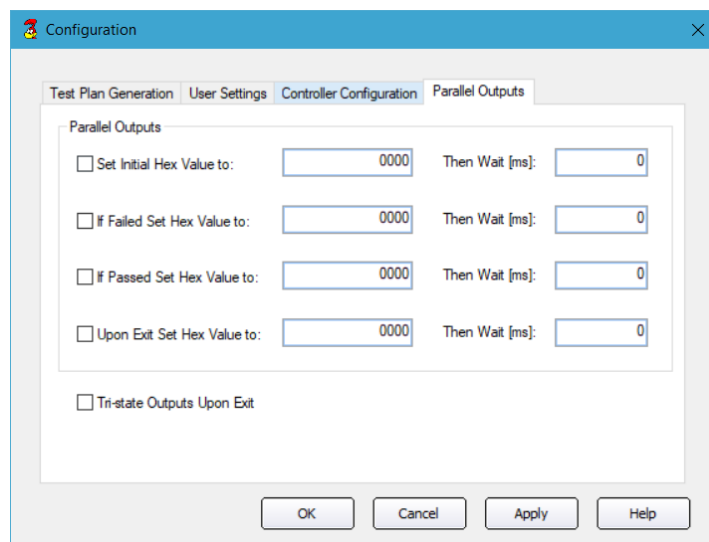


Figure 3-4. NetUSB II Parallel Outputs

Set Initial Hex Value to

Check this box to set the parallel outputs to the specified hex value then pause for the specified number of milliseconds before running a Test Plan.

If Failed Set Hex Value to

Check this box to set the parallel outputs to the specified hex value then pause for the specified number of milliseconds when a Test Plan completes with **Failed** results.

If Passed Set Hex Value to

Check this box to set the parallel outputs to the specified hex value then pause for the specified number of milliseconds when a Test Plan completes with **Passed** results.

Upon Exit Set Hex Value to

Check this box to set the parallel outputs to the specified hex value then pause for the specified number of milliseconds when ScanExpress Runner terminates.

Parallel Output Value Fields

Each TAP of a Corelis high-speed boundary-scan controller supports three individual GPIO (General Purpose I/O) signals. **Error! Reference source not found. Error! Reference source not found.** identifies the mapping of the **Parallel Outputs** window values to the physical pins on the controller. Note that when a Flash Programming (.fpi) test step uses external control signals such as `Write_Strobe*` and/or `Ready_Busy*`, flash control signal functionality takes precedence over values in the **Parallel Outputs** window. It is recommended that the user avoid using these signals to control other functions.

Table 3-11. NetUSB II Parallel Outputs Mapping

Bit	TAP	TAP Pin	Function	Alternate Function
0 Error! Reference	1	11	TAP 1 - GPIO1	<code>Write_Strobe*</code>

Bit	TAP	TAP Pin	Function	Alternate Function
source not found.				
1	1	13	TAP 1 - GPIO2	
2	1	15	TAP 1 - GPIO3	Ready_Busy*
3	2	11	TAP 2 - GPIO1	Write_Strobe*
4	2	13	TAP 2 - GPIO2	
5	2	15	TAP 2 - GPIO3	Ready_Busy*
6	3	11	TAP 3 - GPIO1	Write_Strobe*
7	3	13	TAP 3 - GPIO2	
8	3	15	TAP 3 - GPIO3	Ready_Busy*
9	4	11	TAP 4 - GPIO1	Write_Strobe*
10	4	13	TAP 4 - GPIO2	
11	4	15	TAP 4 - GPIO3	Ready_Busy*

¹ Bit 0 is the least significant bit (LSB).

For example, if the initial hex value is set to “4321” and a NetUSB II controller is being used, GPIO1 of TAP1, GPIO3 of TAP2, GPIO3 of TAP3 and GPIO1 of TAP4 will be driven high and the remaining GPIO signals will be driven low. The most significant digit of the hex value (“4” in this case) is ignored.

Tri-state Outputs Upon Exit

Check this box to tri-state all GPIO pins after setting the exit value when ScanExpress Runner terminates.

Chapter 4: Third Party Application Interface

ScanExpress applications provide general purpose, third-party application programming interfaces (APIs). A “controller specification” string is used to specify the controller and settings when using these APIs. This section clarifies the requirements related to the NetUSB II controller. The examples below reference ScanExpress Runner; please refer to the specific ScanExpress application user’s manual for further information.

Using the NetUSB II with ScanExpress Runner API

The “controller specification” string consists of the name of a Corelis boundary-scan controller followed by a comma-separated list of integer numbers. Each of the numbers represents a selection for different parameters of the specified controller. Please consult the **ScanExpress Runner User’s Manual** for more detail.

Note: The controller specification parameters correspond to the settings on the **Controller Configuration** window of the ScanExpress Runner application graphical user interface.

The relevant Controller Specification String is written to the Runner test plan (.tsp) file for convenience. When using ScanExpress Runner and saving a test plan, the controller specification string is recorded with all parameters as a comment line in the header at the top of the test plan (.tsp) file. Open the .tsp file with your favorite text editor and look for the line that begins with “*ControllerParam*”. This line is write-only and is does not affect controller operation.

The NetUSB II controller uses 32 parameters described in Table 4-1 below.

Controller keyword: **NetUSB II**

Table 4-1. NetUSB II Controller Parameters

Position	Parameter	Value	Setting
1	IP Address	(string)	IP Address (i.e.: 192.168.1.2) or string “USB”
2	TAPs Voltage	1 2 ... 46 47 48	1.00 V 1.05 V ... (0.05 volts per step) 3.25 V 3.30 V Use advanced voltage settings in position 8 through 11
3	Clock Frequency	1 ... 100 ... 109	100 MHz ... (1 MHz increment) 1 MHz ... (0.1 MHz increment) 0.1 MHz
4	TAPs Config	1 2 ... 7 8 9 10	Use TAP1 Use TAP2 ... Use TAP7 Use TAP8 Use TAPs 1 and 2 in series Use TAPs 1, 2, and 3 in series

Position	Parameter	Value	Setting
	
		14	Use TAPs 1 through 7 in series
		15	Use TAPs 1 through 8 in series
5	SPI/I2C TAP Config	1	No direct programming TAP
		2	Use TAP1
		3	Use TAP2
	
		8	Use TAP7
		9	Use TAP8
6	TAPs Off State	1	Active (JTAG signals are driven when tests are not running)
		2	Tri-State
7	Delay Compensation	1	Automatic
		2	No Delay
		3	0.5 Clock Delay
		4	1.0 Clock Delay
		5	1.5 Clock Delay
		6	2.0 Clock Delay
		7	2.5 Clock Delay
		8	3.0 Clock Delay
		9	3.5 Clock Delay
8	TAP1 Voltage	1	1.00 V
		2	1.05 V
	 (0.05 V per step)
		46	3.25 V
		47	3.30 V
9	TAP2 Voltage	1	1.00 V
	 (0.05 V per step)
		47	3.30 V
10	TAP3 Voltage	1	1.00 V
	 (0.05 V per step)
		47	3.30 V
11	TAP4 Voltage	1	1.00 V
	 (0.05 V per step)
		47	3.30 V
12	TAP5 Voltage	1	1.00 V
	 (0.05 V per step)
		47	3.30 V
13	TAP6 Voltage	1	1.00 V
	 (0.05 V per step)
		47	3.30 V
14	TAP7 Voltage	1	1.00 V
	 (0.05 V per step)
		47	3.30 V
15	TAP8 Voltage	1	1.00 V
	 (0.05 V per step)
		47	3.30 V
16	TAP1	1	Automatic

Position	Parameter	Value	Setting
	Input Threshold	2 ... 32	0.50 V ... (0.05 V per step) 2.00 V
17	TAP2 Input Threshold	1 2 ... 32	Automatic 0.50 V ... (0.05 V per step) 2.00 V
18	TAP3 Input Threshold	1 2 ... 32	Automatic 0.50 V ... (0.05 V per step) 2.00 V
19	TAP4 Input Threshold	1 2 ... 32	Automatic 0.50 V ... (0.05 V per step) 2.00 V
20	TAP5 Input Threshold	1 2 ... 32	Automatic 0.50 V ... (0.05 V per step) 2.00 V
21	TAP6 Input Threshold	1 2 ... 32	Automatic 0.50 V ... (0.05 V per step) 2.00 V
22	TAP7 Input Threshold	1 2 ... 32	Automatic 0.50 V ... (0.05 V per step) 2.00 V
23	TAP8 Input Threshold	1 2 ... 32	Automatic 0.50 V ... (0.05 V per step) 2.00 V
24	TAP1 Pinout Configuration	0 324508639 355965919 ... 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* ... (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
25	TAP2 Pinout Configuration	0 324508639 355965919 ... 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* ... (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
26	TAP3 Pinout Configuration	0 324508639 355965919 ... 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* ... (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*

Position	Parameter	Value	Setting
27	TAP4 Pinout Configuration	0 324508639 355965919 ... 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* ... (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
28	TAP5 Pinout Configuration	0 324508639 355965919 ... 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* ... (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
29	TAP6 Pinout Configuration	0 324508639 355965919 ... 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* ... (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
30	TAP7 Pinout Configuration	0 324508639 355965919 ... 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* ... (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
31	TAP8 Pinout Configuration	0 324508639 355965919 ... 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* ... (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
32	TCK Mode	1 2	Gated Continuous

Example

To select the NetUSB II controller using:

- A USB connection
- All TAP voltages set to 3.30 V
- TCK frequency set to 1 MHz
- TAP1 used for JTAG
- TAP2 used for direct SPI/I2C programming
- Tri-state the JTAG signal when test is finished
- Automatic delay compensation
- Automatic input threshold
- Default pinout

To configure the NetUSB II for these options, use this “controller specification” string:

```
-controller "NetUSB-II,USB,47,31,1,3,2,1,47,47,47,47,47,47,47,47,1,1,1,1,1,1,1,1,324508639,324508639,324508639,324508639,324508639,324508639,324508639,324508639,1,"
```

Note: The pinout configuration value in decimal format represents the encoded pin Numbers for the JTAG, SPI, or I²C signals. Each digit of the value in hex format corresponds to the pin number of the signals.

Table 4-2. Pinout Values

Hex Digits	1st	2nd	3rd	4th	5th	6th	7th	8th
JTAG	TRST	TDI	TDO	TMS	TCK	IO1	IO2	IO3
SPI	SCK	MOSI	MISO	CS0	CS1	CS2	CS3	CS4
I2C	SDA	SCL	-	-	-	-	-	-

For example, the standard pinout configuration for JTAG is:

```
[Signal:Pin#] = [TRST:1] [TDI:3] [TDO:5] [TMS:7] [TCK:9] [IO1:11] [IO2:13] [IO3:15]
```

This would be represented as:

```
0x13579BDF (324508639 in decimal format)
```

The custom pinout configuration of

```
[Signal:Pin#] = [TRST:1] [TDI:5] [TDO:7] [TMS:9] [TCK:3] [IO1:11] [IO2:13] [IO3:15]
```

would be represented as:

```
0x15793BDF (360266719 in decimal format)
```

If an invalid number is used, the configuration will be set to the standard pinouts by default. Therefore, if you want to use the standard pinout configuration, you may just use the value "0" instead of "324508639".

Using the NetUSB II with the Scan Function Library

The **Scan Function Library (SFL)** is a C interface to Corelis boundary-scan controllers which allows users to perform data and instruction scans via the IEEE Standard 1149.1 test bus. Consult the **NetUSB II SFL User's Manual** for more details on using the NetUSB II SFL.

Chapter 5: Recommended Target Connectors

10-pin TAP Connector

The Boundary-Scan TAP is a well-defined IEEE-1149.1-compatible electrical interface between boundary-scan test equipment and the boundary-scan compatible devices in the user's target board. Boundary-scan based test equipment, such as the Corelis ScanExpress family of products, utilize one or more TAPs to interface to the UUT. This section explains how to design in a simple TAP connector for your target that is compatible with most standard test equipment. The cables provided with the NetUSB II provide a connector compatible with this standard.

The controller TAP contains 5 signals: TCK, TMS, TDO, TDI and TRST*. It also contains ground signal(s). Corelis recommends the standard TAP connector shown in Figure 5-1, which is widely regarded as the industry standard.

Note: Corelis recommends that each signal be terminated with a resistor to improve noise immunity.

The connector on the user's target should have a standard flat cable compatible pin-out to match the TAP connector described in Table 5-1. Figure 5-1 shows the top component-side view of the basic target 10-pin connector header (0.100 × 0.100 in. spacing).

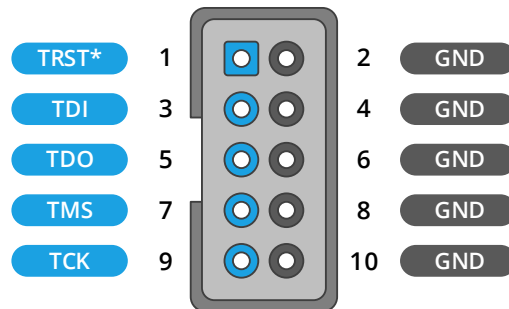


Figure 5-1. Standard 10-pin TAP Connector (top view)

Table 5-1 describes the 10-pin TAP connector signals and the Corelis recommended values of terminating resistors.

Table 5-1. 10-pin TAP Signal Description and Termination

Pin	Signal	Direction	Recommended Termination
1	TRST*	Input to the UUT	4.7 k Ω pull-up
2	GND		
3	TDI	Input to the UUT	4.7 k Ω pull-up
4	GND		
5	TDO	Output of the UUT	33 Ω series
6	GND		
7	TMS	Input to the UUT	4.7 k Ω pull-up
8	GND		
9	TCK	Input to the UUT	4.7 k Ω pull-up
10	GND		

Note: Some target boards may require a pull-down resistor on the TRST* signal to ensure normal device operations when not in boundary-scan test mode.

Table 5-2 summarizes the specifications for the 10-pin TAP connector. Equivalent connectors are available from other manufacturers.

Table 5-2. Standard 10-Pin TAP Connector

Reference	Description	Manufacturer	Part Number
10-Pin Target TAP	Straight header, 10-pin, 4-wall, with center notch	3M	3473-6610

Figure 5-2 shows a typical schematic of the target TAP connector with the recommended termination resistors. The 4.7 k Ω pull-up resistors should connect to the target V_{cc} supply corresponding to the boundary-scan device interface voltage (programmable on the NetUSB II controller from 1.00 V to 3.30V). Recommended resistor values are $\pm 5\%$. Good design practices specific to the UUT and the device manufacturer recommendations take precedence over Corelis recommended values.

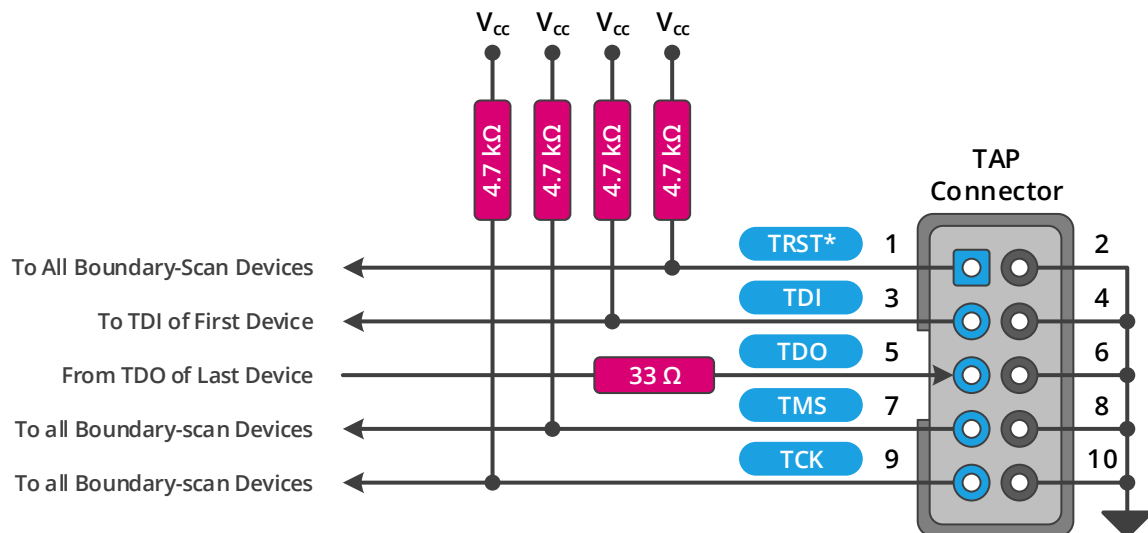


Figure 5-2. 10-pin TAP Connector Schematic

16-pin Flash Programming TAP Connector

To support expedited in-circuit programming of flash or microprocessor devices, Corelis recommends including supplemental control signals in the TAP interface. These will exploit the Corelis controllers' advanced methods to accelerate the target device programming session. The ScanExpress Programmer, for example, can use the added signals of a 16-pin TAP, like Figure 5-3, to improve programming time. Cables complying with this topology are available for the NetUSB II hardware.

This interface adds `Write_Strobe*`, `Ready_Busy*`, and additional ground signals to the standard 5-signal interface. Using the termination resistors recommended in Table 5-4 below can further improve signal quality.

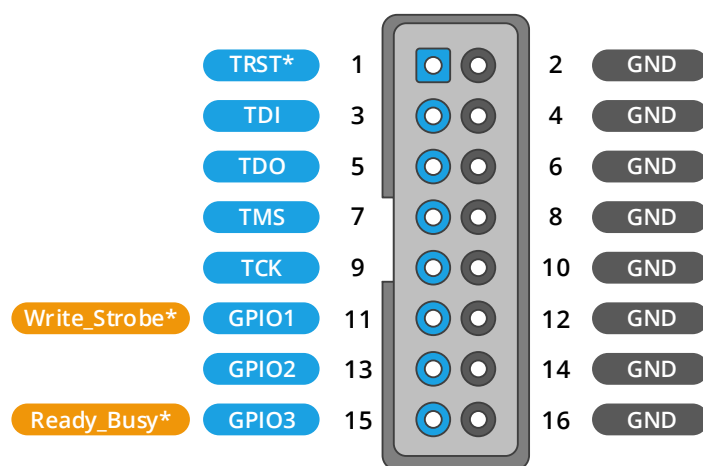


Figure 5-3. Boundary-scan Flash Programming 16-pin TAP Connector (top view)

Corelis flash programming software supports the external signals `Write_Strobe*` and `Ready_Busy*`, while still offering the standard—but slower—fully scanned out/in signals approach.

The `Write_Strobe*` signal is active low and should be pulled up with a 4.7 k Ω resistor on the target board. It should be logically *OR-ed* with the flash Write-Enable (`WE*`) signal and both inputs to the *OR* should be pulled up. This way either the target's flash `WE*` signal or the controller's external `Write_Strobe*` going low will assert the flash `WE*` input.

The active low `Ready_Busy*` signal is typically an open-collector/open-drain signal that ties directly to the same signal(s) on the flash device(s). This enables multiple devices to drive it toward the NetUSB II controller.

Table 5-3 summarizes the specifications for a 16-pin TAP connector without latch ejector. Equivalent connectors are available from other manufacturers.

Table 5-3. Flash Programming TAP 16-Pin Connector

Reference	Description	Manufacturer	Part Number
Flash TAP	Straight header, 16-pin, 4 wall, with center notch	3M	2516-6002UG

Table 5-4 describes the signals and Corelis recommended values of terminating resistors for a 16-pin TAP connector.

Table 5-4. 16-pin TAP Signal Description and Termination

Pin	Signal	Direction	Recommended Termination
1	TRST*	Input to the UUT	4.7K pull-up
2	GND		
3	TDI	Input to the UUT	4.7K pull-up
4	GND		
5	TDO	Output from UUT	33 Ω series
6	GND		
7	TMS	Input to the UUT	4.7K pull-up
8	GND		
9	TCK	Input to the UUT	4.7K pull-up
10	GND		
11	Write_Strobe*	Input to the UUT	4.7K pull-up
12	GND		
13	Reserved		
14	GND		
15	Ready_Busy*	Output from UUT	4.7K pull-up
16	GND		

Note: Some target boards may require a pull-down resistor on the TRST* signal to assure normal device operations when not in boundary-scan test mode.

Figure 5-4 shows a typical schematic of the target TAP connector with termination resistors. The 4.7 k Ω pull-up resistors should connect to the target V_{cc} supply corresponding to the boundary-scan device interface voltage (programmable on the NetUSB II controller from 1.00 V to 3.30 V). Recommended resistor values are $\pm 5\%$. Good design practices specific to the UUT and the device manufacturer recommendations take precedence over Corelis recommended values.

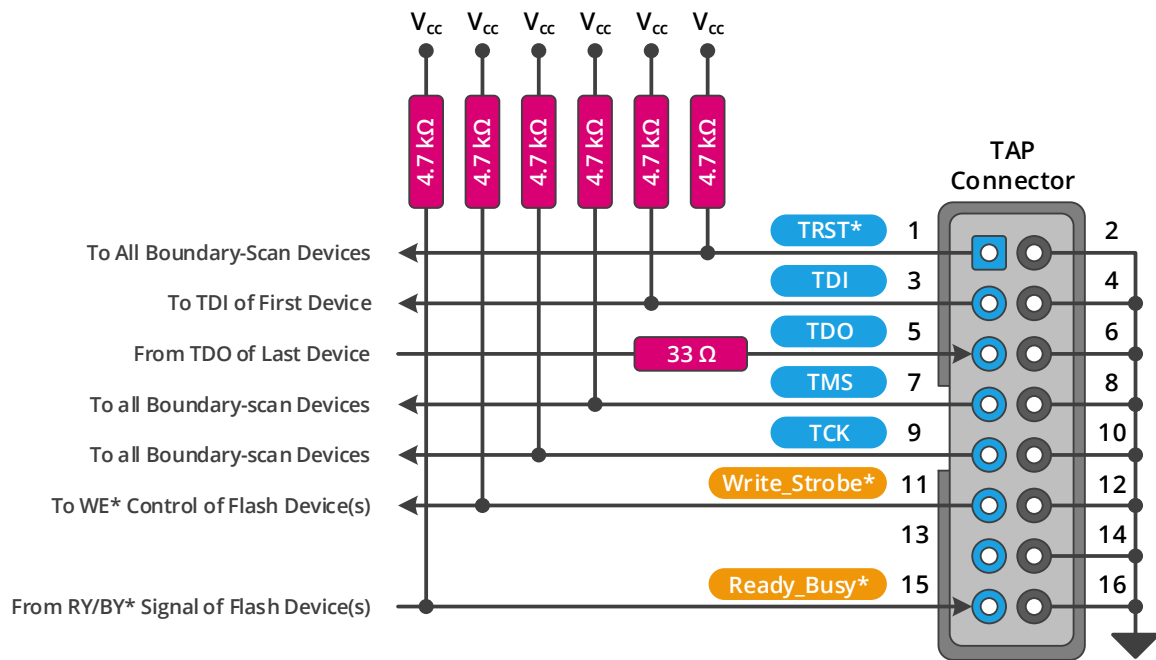


Figure 5-4. 16-pin Flash Programming TAP Connector Schematics

20-pin Flash Programming & Power Test TAP Connector

To support expedited in-circuit programming of flash or microprocessor devices, Corelis recommends including supplemental control signals in the TAP interface. These will exploit the Corelis controllers' advanced methods to accelerate the target device programming session. The ScanExpress Programmer, for example, can use the added signals of a 20-pin TAP, similar to Figure 5-5 below, to improve programming time. Cables complying with this topology are available for the NetUSB II hardware.

This interface adds `Write_Strobe*`, `Ready_Busy*`, and two power test point pins as well as additional ground signals to the standard 5-signal interface. Terminating resistors (see Table 5-5) can further improve signal quality.

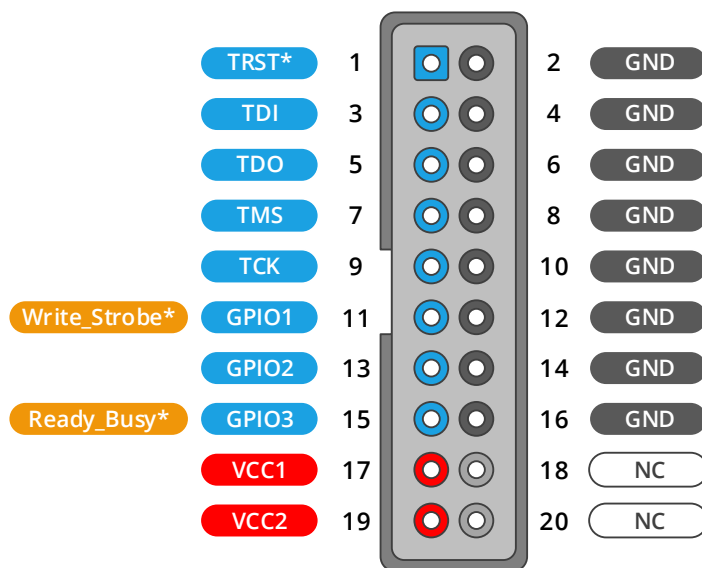


Figure 5-5. Boundary-scan Flash Programming with Power Test Points 20-pin TAP Connector (top view)

Corelis' Flash Programming software supports the external signals `Write_Strobe*` and `Ready_Busy*`, while still offering the standard, but slower, fully scanned out/in signals approach.

The `Write_Strobe*` signal is active low and should be pulled up with a 4.7 kΩ resistor on the target board. It should be logically *OR-ed* with the flash Write-Enable (WE*) signal. This way either the target's flash WE* signal or the controller's external `Write_Strobe*` going low will assert the flash WE* input.

The active low `Ready_Busy*` signal is typically an open-collector/open-drain signal that ties directly to the same signal(s) on the flash device(s). This enables multiple devices to drive it toward the NetUSB II controller.

Table 5-5 summarizes the specifications for a 20-pin TAP connector without latch ejector. Equivalent connectors are available from other manufacturers.

Table 5-5. Flash Programming TAP 20-pin Connector

Reference	Description	Manufacturer	Part Number
Flash TAP	Straight header, 20-pin, 4 wall, with center notch	3M	2516-6002UG

Table 5-6 describes the signals and Corelis recommended values of terminating resistors:

Table 5-6. 20-pin TAP Signal Description and Termination

Pin	Signal	Direction	Termination
1	TRST*	Input to the UUT	4.7 k Ω pull-up
2	GND		
3	TDI	Input to the UUT	4.7 k Ω pull-up
4	GND		
5	TDO	Output from UUT	33 Ω series
6	GND		
7	TMS	Input to the UUT	4.7 k Ω pull-up
8	GND		
9	TCK	Input to the UUT	4.7 k Ω pull-up
10	GND		
11	Write_Strobe* / GPIO1	Input to the UUT	4.7 k Ω pull-up
12	GND		
13	GPIO2	Input to the UUT	4.7 k Ω pull-up
14	GND		
15	Ready_Busy* / GPIO3	Output from UUT	4.7 k Ω pull-up
16	GND		
17	VCC1	Power Test Point	None
18	NC	No Connect	None
19	VCC2	Power Test Point	None
20	NC	No Connect	None

Figure 5-6 below shows a typical schematic of the target TAP connector with termination resistors. The 4.7 k Ω pull-up resistors should connect to the target V_{cc} supply corresponding to the boundary-scan device interface voltage (programmable on the NetUSB II controller from 1.00 V to 3.30 V). Recommended resistor values are $\pm 5\%$. Good design practices specific to the UUT and the device manufacturer recommendations take precedence over Corelis recommended values.

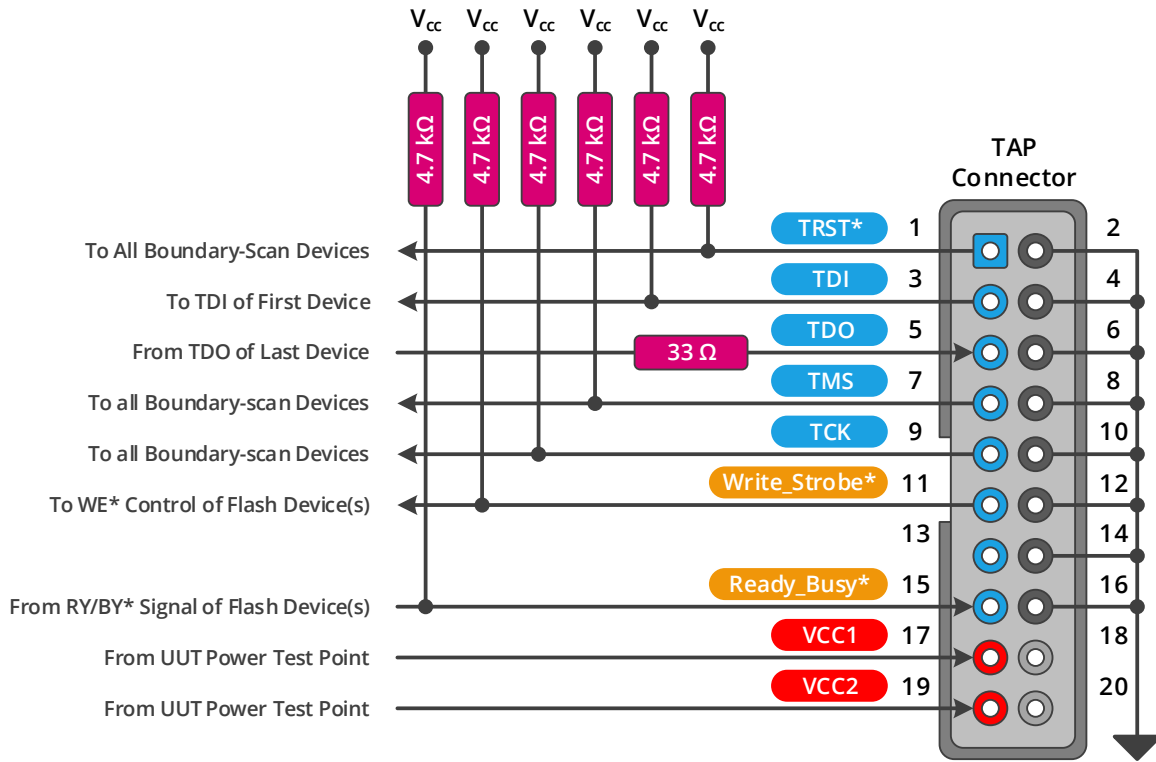


Figure 5-6. 20-pin Flash Programming with Power Test Points Connector Schematics

Direct I2C Direct Programming Connector

The default pinout for Direct I2C Programming is shown in Table 5-7 below.

Table 5-7. I2C Signal Description and Recommended Termination

Pin	Signal	Direction	Termination
1	SDA	Bidirectional	1 k Ω pull-up
2	GND		
3	SCL	Input to the UUT	1 k Ω pull-up
4	GND		

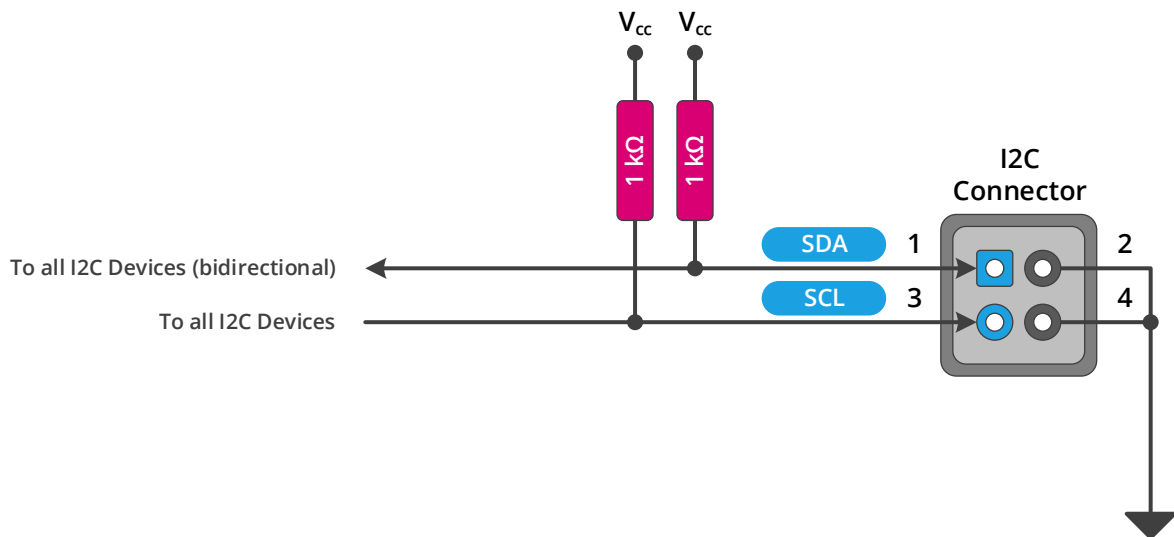


Figure 5-7. Direct I2C Programming Connector Schematics

Direct SPI Programming Connector

The default pinout for Direct SPI Programming is shown in Table 5-8 below.

Table 5-8. SPI Signal Description and Recommended Termination

Pin	Signal	Direction	Termination
1	SCK	Input to the UUT	4.7 k Ω pull-up
2	GND		
3	MOSI	Input to the UUT	4.7 k Ω pull-up
4	GND		
5	MISO	Output from UUT	33 Ω series
6	GND		
7	CS0*	Input to the UUT	4.7 k Ω pull-up
8	GND		
9	CS1*	Input to the UUT	4.7 k Ω pull-up
10	GND		
11	CS2*	Input to the UUT	4.7 k Ω pull-up
12	GND		
13	CS3*	Input to the UUT	4.7 k Ω pull-up
14	GND		
15	CS4*	Input to the UUT	4.7 k Ω pull-up
16	GND		

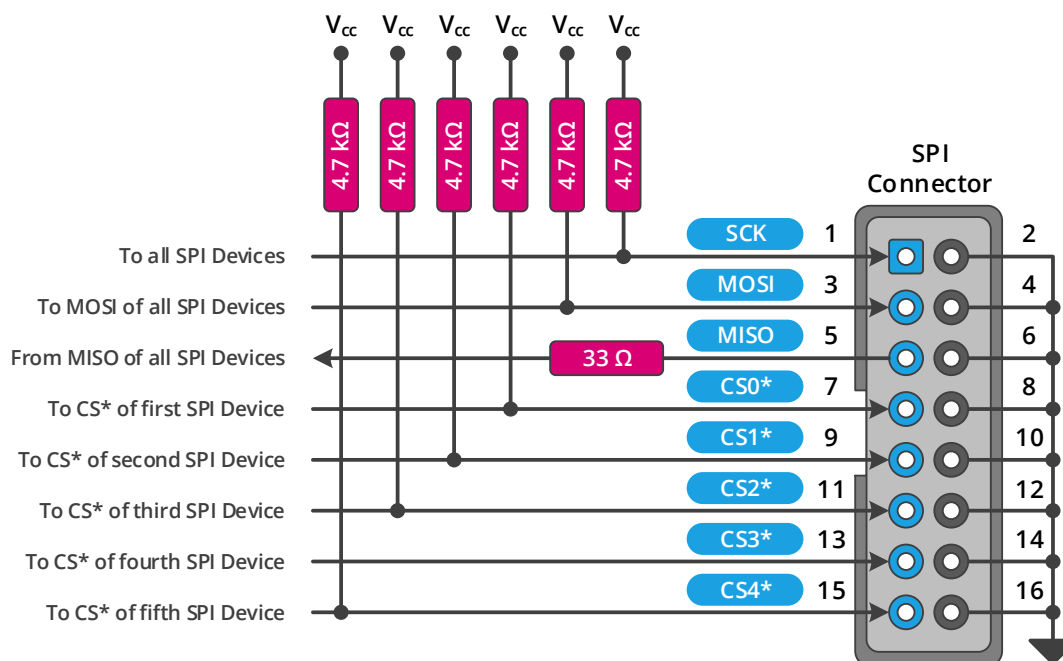


Figure 5-8. SPI Direct Programming Connector Schematics

Chapter 6: Self-Test Application

Overview

A self-test application is provided to run basic trouble-shooting diagnostics on the hardware.

Loopback Cables

The self-test includes an optional loopback capability to verify proper operation of the TAP signals.

Connect 1:1 20-pin cables (Corelis P/N 15466) between the TAPs shown in Table 6-1 or disable the loopback test steps.

Table 6-1. Self-Test Loopback Cable Connections.

Connection 1	Connection 2	NetUSB II 4-TAP	NetUSB II 8-TAP
TAP 1	TAP 3	x	x
TAP 2	TAP 4	x	x
TAP 5	TAP 7	n/a	x
TAP 6	TAP 8	n/a	x

Note: Disconnect any other targets as they will interfere with the self-test.

Running the Test

The self-test application is installed in the same folder as the ScanExpress Applications (ScanExpress Runner, ScanExpress Debugger and ScanExpress Programmer).

1. Connect the NetUSB II to an available USB or Ethernet port.
2. Connect the power adapter to the NetUSB II power connected labeled **12V DC** and plug the power adapter into an electrical outlet.
3. Toggle the switch labeled **Power** to the **ON** position. Wait approximately 30 seconds for the Status LED stops blinking.
4. Execute “**NetUSB_II_SelfTest.exe**” from “**C:\Program Files (x86)\Common Files\Coreelis Shared\12.0**”.
5. Select **USB** or **Net** (and enter the IP Address).
6. Enable or disable the “**Loopback Test**”.
7. Click **Run**.

The program should respond with results similar to those shown in Figure 6-1.

The screenshot displays the 'NetUSB II Self Test Application (v0.25)' window. It is divided into several sections:

- UUT Information:** This section contains fields for device identification. The 'USB' radio button is selected. The IP Address is '192.168.1.180'. The Firmware Version is 'NetUSB II Win32 SFL DLL v0.99, Firmware : 0.42, FPGA Version : 5'. The MAC Address is 'B0:D5:CC:C4:99:4B'. There are also fields for MB PCBA Part Number (ASF4100001), JTAG 0 PCBA Part Num (ASF4080001), JTAG 1 PCBA Part Num, MB PCBA Part Revision (2), JTAG 0 PCBA Part Rev (1), JTAG 1 PCBA Part Rev, MB PCBA Serial Number (16186745), JTAG 0 Serial Number (16186709), JTAG 1 Serial Number, Assembly Part Number, Assembly Part Revision, and Assembly Serial Number.
- Test Results:** This section shows the outcomes of various tests. On the left, 'Memory Test', 'Firmware Integrity', 'PMIC Power Controller Test', 'ATmega Reset Controller Test', and 'Fan Controller Test' all show 'PASSED'. On the right, 'I2C Switch Test', 'Temperature Sensor Test', and 'ADC Test' also show 'PASSED'. The 'Loopback Test' section has four checked options: 'TAP1 & TAP3', 'TAP2 & TAP4', 'TAP5 & TAP7', and 'TAP6 & TAP8', each with a corresponding 'PASSED' result.
- Buttons:** At the bottom right, there are three buttons: 'Open Log Folder', 'Run', and 'Close'.

Figure 6-1. NetUSB II Self-Test Results

Chapter 7: Firmware Update Utility

Overview

The NetUSB II includes field-upgradable firmware. A firmware update utility is included with ScanExpress Tools and the Scan Function Library CD.

Note: The firmware should not normally need to be modified unless the ScanExpress application or a Corelis support engineer asks you to do so.

Updating the Firmware

The firmware update utility is installed by with the ScanExpress CD or the Boundary-Scan Tools CD. The “\Firmware\NetUSB II” subdirectory contains the update utility and the new firmware file.

1. Execute “C:\Program Files (x86)\Corelis\ScanExpress Runner v6\Firmware\NetUSB II\NetUSB-II_Flash.exe”. The Corelis NetUSB II Firmware Update Utility shown in Figure 7-1 below will be displayed.

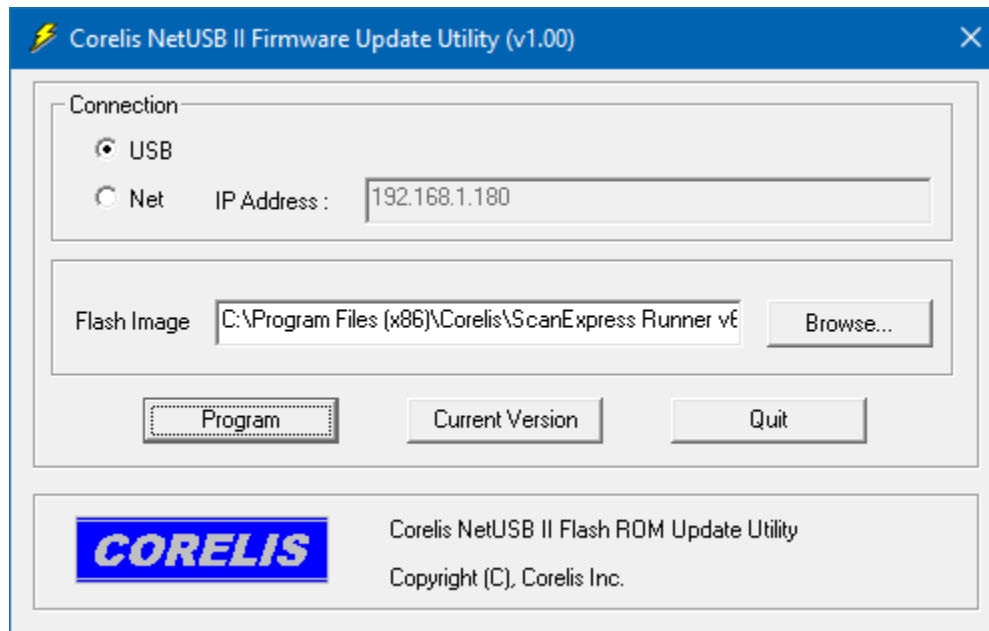


Figure 7-1. NetUSB II Firmware Update Utility

2. Select **USB** or **Net** (and enter the IP Address).
3. Click the **Browse** button and select the new firmware flash image file (.frm).
4. Click the **Program** button to start updating the firmware. The application will ask for a confirmation to proceed, as shown in Figure 7-2 below.

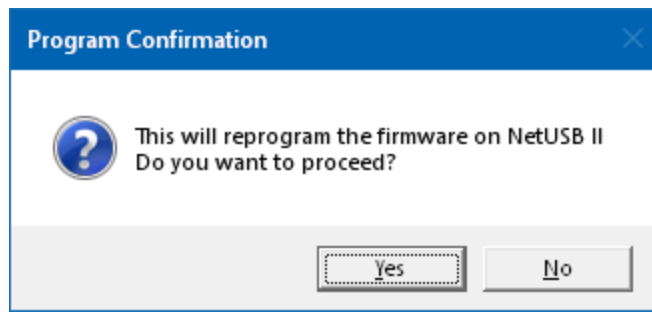


Figure 7-2. Firmware Update Confirmation Dialog

5. Click **Yes** to start the update process. The utility will show a progress bar while updating the firmware.

Note: Do not power off the unit or disconnect the Ethernet/USB cable until the firmware update process is complete.

6. When finished a dialog box will appear. Click **OK**.

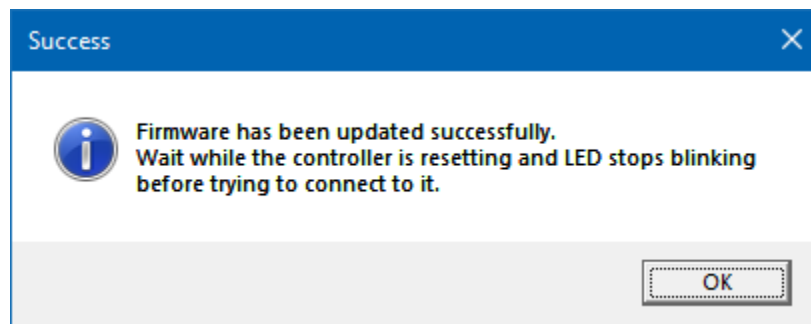


Figure 7-3. Firmware Update Success Dialog

7. Close the firmware update utility and cycle power on the NetUSB II unit.

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Version 2, June 1991

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