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PXIE-1149.1/4E

PXIE-1149.1/4E

High-Speed PXIE Boundary-Scan Controller

User's Manual

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PRINTING HISTORY

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Chapter 1:
Product Overview

Introduction

The PXIE-1149.1/4E High-Speed Boundary-Scan (JTAG) Controller is a member of the Corelis ScanExpress™ family of scan-based test, analysis, and diagnostic tools. The PXIE-1149.1/4E interfaces between a PC equipped with a PXIE bus and any IEEE Standard 1149.1 compatible target. The PXIE-1149.1/4E is designed to control the operation of an IEEE Standard 1149.1 boundary-scan (JTAG) test access port (TAP) by generating the proper signals under software control to interface with the target device. It contains memory-behind-the-pin architecture and supports scan operations at continuous JTAG clock (TCK) speeds of up to 75 MHz.

Figure 1-1. PXIE-1149.1/4E Boundary-scan Controller

What is IEEE Standard 1149.1?

The PXIE-1149.1/4E facilitates software-controlled boundary-scan operations per IEEE Standard 1149.1. It provides command access to the target's Test Access Port (TAP), accessing device internal registers and on-chip debugger, verifying PCB interconnects, performing functional testing and debug, without manual probing. The JTAG interface also provides access to internal device functions that are not accessible via external probing, thus enabling fault isolation within the device itself. The JTAG interface also enables programming target Flash and CPLD devices, as well as data download and uploading to and from the target memory devices.

The PXIE-1149.1/4E is often used to perform microprocessor emulation via the device JTAG port. It is used for firmware development providing single-step, break, and content update/visibility access.

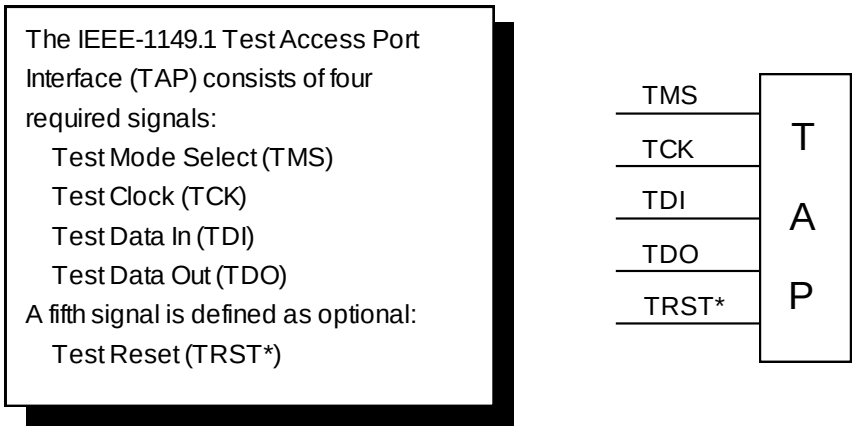


Figure 1-2. Minimal Test Access Port

Features of the PXIE-1149.1/4E

The Corelis PXIE-1149.1/4E is a sophisticated test controller that can access devices, boards or systems that are compliant with IEEE Standard 1149.1. The PXIE bus-compatible card supports up to four JTAG boundary-scan chains (TAPs). In addition, three general purpose, bi-directional discrete I/O signals per TAP can test or control non-boundary-scan areas of the unit under test (UUT). The discrete I/O signals can also assist in greatly expediting certain long scan activities, such as Flash programming. With its software-controlled voltage translating logic for all the above signals, the PXIE-1149.1/4E can test low-voltage systems.

The PXIE-1149.1/4E also contains several performance enhancing functional sections aimed at streamlining test vector throughput and emulator target download/upload transfers. Key functional elements include the TAP controller, and the memory resources that support it. The on-board memory provides scan data buffering and can at times store the entire scan data for maximum performance, real-time scan operations.

A test system operates the TAP controller and its associated memory through the host PXIE Port, while the Test Clock (TCK) rate can operate up to 100 MHz depending on selected signal voltages and target conditions. The on-board memory elements further decouple the scan operations from the host software. A hardware state machine that contains status and control registers accessible through the PCIE interface directly controls all functions of the PXIE-1149.1/4E.

Hardware mechanisms enable optimal data flow between the PCIE port and the memory resources paced by the port and/or scanning rates underway, in both directions.

A programmable, time-delay skew compensation mechanism supports the PXIE-1149.1/4E's high TCK rates. It accommodates the returned, target scan stream-delays due to signal travel time down and up the cable. It can also adjust for a target's internal TCK-to-TDO response delay.

Adjustable Voltage Levels

The software-programmable voltage level of the TAP interfaces and discrete I/O can be set to any voltage between 1.25 V and 3.30 V in increments of about 0.05V. Each of the four TAPs has its own programmable voltage settings.

Discrete Input/Output Signals

The PXIE-1149.1/4E operates three discrete input/output signals under software control. These attach to the target TAP connector. They are driven or sensed as directed by software, in coordination with the scanning operation. Each signal can be configured independently as TTL output, open-collector (open-drain) output, or as input at the programmable voltage level. As open-collector drivers, they can readily tie to similar target signals without the need to alter its circuitry, yet still gain control of related functions, such as a Flash write signal.

As outputs, these discrete signals are useful for providing control functions on the user target system such as general reset, power control, device write pulse, disable/enable and/or similar signals for non-boundary-scan target stimulus.

Conversely, as inputs, they enable host sensing of the target to pace scanning activity or related conditions (such as a Flash ready signal).

PXIE Interface

The PXIE-1149.1/4E is a PXI peripheral module that fits in a 3U slot utilizing 1 lane of PCIe. This PXI interface supplies the power to operate the PXIE-1149.1/4E. The PXIE-1149.1/4E is not hot pluggable. Power should be off while install and removing the PXIE-1149.1/4E controller.

Programmable Clocks

The PXIE-1149.1/4E's programmable TCK output to the IEEE Standard 1149.1 compatible target system can be configured over a wide range of frequencies, using on-board clock-generation circuitry. A programmable Phase Locked Loop (PLL) enables a wide range as well as fine- selection resolution. See Table 1-1 for the set of programmable values.

TCK range (MHz)	Rate Resolution (MHz)
15 to 75	1
1 to 15	0.5
0.05 to 1	0.05

Table 1-1. Programmable TCK Frequencies

Controllable Slew Rate

The PXIE-1149.1/4E supports slow or fast slew rate on the outputs.

Software Pin Configuration

The PXIE-1149.1/4E's pins are remappable in the ScanExpress software.

Pin Protection

The PXIE-1149.1/4E features voltage-detection circuitry to prevent the drivers from being damaged if the outputs are inadvertently shorted to power or ground.

PXIE-1149.1/4E Hardware Specifications

Physical

Mechanical Dimensions (box)	8.5 inches x 0.8 inches x 5.1 inches (+/- 0.25")

Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing

Storage Environment

Temperature	-40°C to 85°C

Host Interface

PXI interface	3U slot using 1 lane of PCIE.
Required Host CPU	Pentium III @ 1GHz or better
Required Operating System	Windows 7, Windows 10

Power Requirements

12V, 3.3V	Provided by the PXI interface. No external power supply needed.

PXIE-1149.1/4E Electrical Specifications

JTAG TAP Interface

PXIE-1149.1/4E TAP Connectors	20-pin (2x10) IDC header (0.050” x 0.100"), AMP/Tyco part number 5-104069-1
PXIE-1149.1/4E TAP Connector Mating Connectors	20-pin (2x10) IDC receptacle (0.050” x 0.100"), AMP/Tyco part number 1-111196-8 or equivalent
Minimum TCK Frequency	0.05 MHz
Maximum TCK Frequency	75 MHz
TCK Frequency Steps	0.05 MHz increments between 0.05 and 1 MHz 0.50 MHz increments between 1 and 15 MHz 1.0 MHz increments between 15 and 75 MHz
Maximum scanning data length	unlimited
Programmable Voltage (V_adj) Range	1.25V to 3.3V in 0.05V steps

Symbol	Test Conditions	Limit Min	Limit Max	Units
V_{IH}	V_adj >= 2.7 V	2	V_adj + 0.5	V
	V_adj < 2.7 V	0.65 × V_adj	V_adj + 0.5	V
V_{IL}	V_adj >= 2.7		0.8	V
	V_adj <= 2.0		0.35 × V_adj	V
V_{OH}	I_{OH}= -12 mA	V_adj – 0.5		V
V_{OL}	I_{OL} = 12 mA		0.4	V

Table 1-2. PXIE-1149.1/4E DC and Switching Characteristics

Chapter 2:
PXIE-1149.1/4E Installation

Installing the ScanExpress software and PXIE-1149.1/4E hardware

The PXIE-1149.1/4E product consists of the following components:

- PXIE-1149.1/4E Hardware
- PXIE-1149.1/4E User's Manual
- One 80-pin to Four 20-pin TAP Cable, Corelis P/N 15467

Please ensure that all items listed above are present and free from visible damage or defects before proceeding. If anything appears to be missing or damaged, immediately contact Corelis at the number shown on the title page of this manual.

Software Must Be Installed.

The PXIE-1149.1/4E installation procedure requires the use of software that contains the driver for the PXIE-1149.1/4E module. Obtain the ScanExpress CD-ROM (or any other Corelis application that supports the PXIE-1149.1/4E module) in order to proceed with installation. Install the PXIE-1149.1/4E controller before installing the ScanExpress Application Software.

PXIE-1149.1/4E Hardware Installation

To install the PXIE-1149.1/4E on a host PC, follow the installation steps below. Plug in the PXIE-1149.1/4E controller into an available PXIE port on the host PC while powered down. The following section describes this process in detail for installing using Windows 7 and Windows 10. Note that depending on the version of Windows used, the procedure may differ slightly.

Installation Steps

1. While powered down, install the PXIE-1149.1/4E module into the any available PXIE peripheral slot. Then power on.
2. Install the application software, such as "ScanExpress Runner," from the CD on your computer.

3. The **Found New Hardware Wizard** dialog box will automatically start as shown below in Figure 2-1.
4. Select "**No, not this time**" as shown below and click on the Next button.

Figure 2-1. Found New Hardware Wizard

5. The following dialog box as shown in Figure 2-2 will pop up. Select "**Install the software automatically (Recommended)**" and click on the **Next** button.

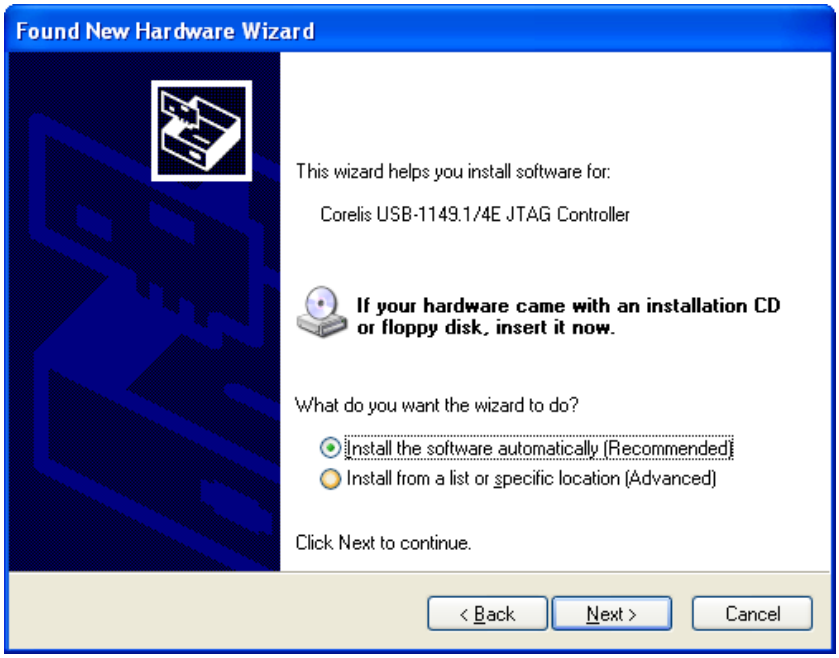


Figure 2-2. Found New Hardware Wizard

6. After the necessary files are copied to the system, the following dialog box, Figure 2-3, will pop up indicating that the device driver is successfully installed.

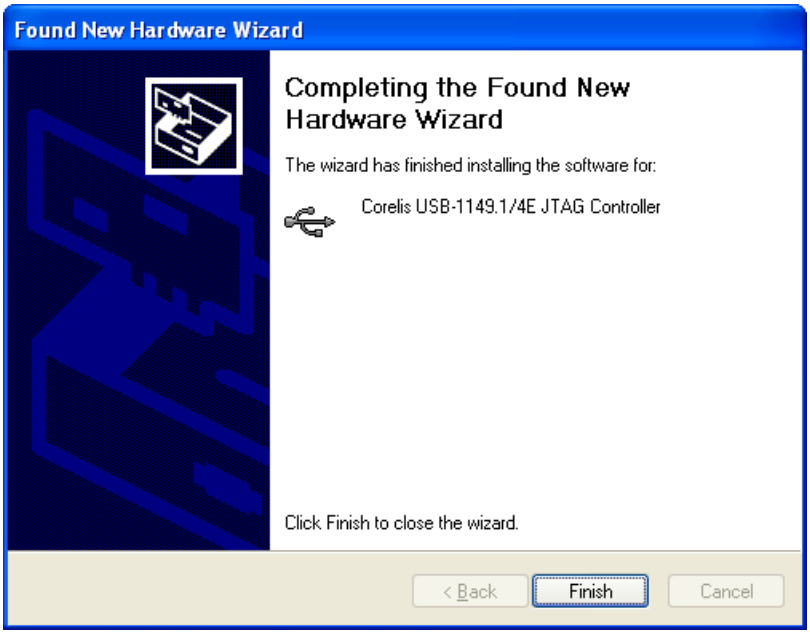


Figure 2-3. Installation Successfully Completed

7. Click on the **Finish** button to close the dialog box.
8. The installation of the device drivers is now completed. Verify that the PXIE-1149.1/4E is correctly installed by checking for its entry in the **Windows Device Manager**. To run the Device Manager, right-mouse click on the **My Computer** icon and then select **Properties**. Choose the **Hardware** tab and click on the **Device Manager** button. Corelis **USB-1149.1/4E JTAG Controller** should be listed in the **Universal Serial Bus controller** section as shown in **Figure 2-4**.

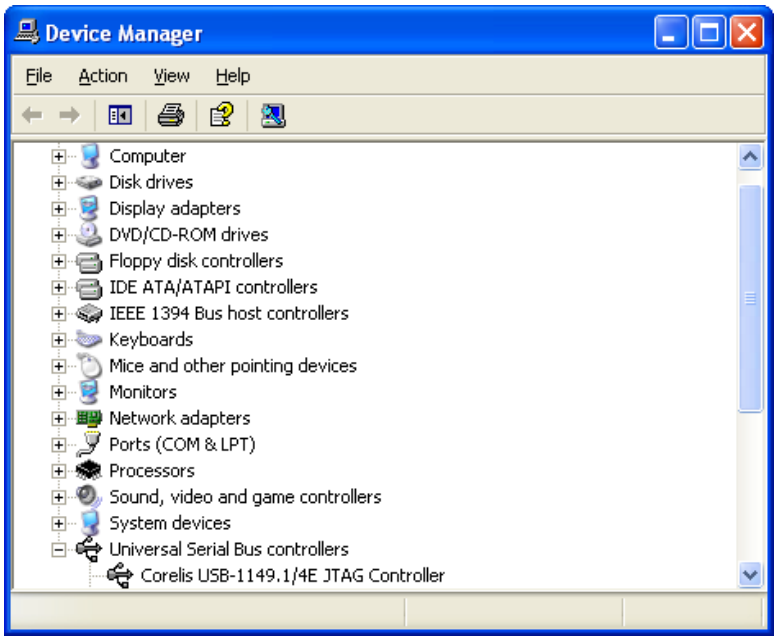


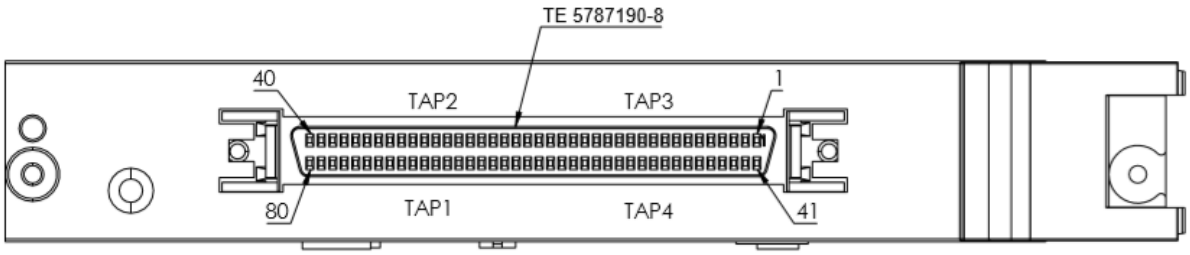
Figure 2-4. Windows Device Manager

Congratulations! The PXIE-1149.1/4E drivers have now been successfully installed on your computer and the controller is now ready to be used. We suggest that you preserve the original packing material for the future shipment or storage of the PXIE-1149.1/4E.

Chapter 3:
Connecting to the Target

Connecting to the Target

The connection to the target board/system is through the TAP connectors on the front of the PXIE-1149.1/4E. Figure 3-1 shows the front view of the PXIE-1149.1/4E box, including the four TAP connectors, which are clearly marked on the cable: TAP 1, TAP 2, TAP 3 and TAP 4.



Pin	Signal Name	Signal Description
1	TAP3 TRST*	Test Reset (Input to the UUT)
2	TAP3 GND	
3	TAP3 TDI	Test Data In (Input to the UUT)
4	TAP3 GND	
5	TAP3 TDO	Test Data Out (Output from the UUT)
6	TAP3 GND	
7	TAP3 TMS	Test Mode Select (Input to the UUT)
8	TAP3 GND	
9	TAP3 TCK	Test Clock (Input to the UUT)
10	TAP3 GND	
11	TAP3 IO1	Discrete Input/Output to the UUT
12	TAP3 GND	
13	TAP3 IO2	Discrete Input/Output to the UUT
14	TAP3 GND	
15	TAP3 IO3	Discrete Input/Output to the UUT
16	TAP3 GND	
17	Reserved	Do Not Connect
18	Reserved	Do Not Connect
19	Reserved	Do Not Connect
20	Reserved	Do Not Connect
21	TAP2 TRST*	Test Reset (Input to the UUT)
22	TAP2 GND	
23	TAP2 TDI	Test Data In (Input to the UUT)
24	TAP2 GND	
25	TAP2 TDO	Test Data Out (Output from the UUT)
26	TAP2 GND	
27	TAP2 TMS	Test Mode Select (Input to the UUT)
28	TAP2 GND	
29	TAP2 TCK	Test Clock (Input to the UUT)
30	TAP2 GND	
31	TAP2 IO1	Discrete Input/Output to the UUT
32	TAP2 GND	
33	TAP2 IO2	Discrete Input/Output to the UUT
34	TAP2 GND	
35	TAP2 IO3	Discrete Input/Output to the UUT
36	TAP2 GND	
37	Reserved	Do Not Connect
38	Reserved	Do Not Connect
39	Reserved	Do Not Connect
40	Reserved	Do Not Connect

Pin	Signal Name	Signal Description
41	TAP4 TRST*	Test Reset (Input to the UUT)
42	TAP4 GND	
43	TAP4 TDI	Test Data In (Input to the UUT)
44	TAP4 GND	
45	TAP4 TDO	Test Data Out (Output from the UUT)
46	TAP4 GND	
47	TAP4 TMS	Test Mode Select (Input to the UUT)
48	TAP4 GND	
49	TAP4 TCK	Test Clock (Input to the UUT)
50	TAP4 GND	
51	TAP4 IO1	Discrete Input/Output to the UUT
52	TAP4 GND	
53	TAP4 IO2	Discrete Input/Output to the UUT
54	TAP4 GND	
55	TAP4 IO3	Discrete Input/Output to the UUT
56	TAP4 GND	
57	Reserved	Do Not Connect
58	Reserved	Do Not Connect
59	Reserved	Do Not Connect
60	Reserved	Do Not Connect
61	TAP1 TRST*	Test Reset (Input to the UUT)
62	TAP1 GND	
63	TAP1 TDI	Test Data In (Input to the UUT)
64	TAP1 GND	
65	TAP1 TDO	Test Data Out (Output from the UUT)
66	TAP1 GND	
67	TAP1 TMS	Test Mode Select (Input to the UUT)
68	TAP1 GND	
69	TAP1 TCK	Test Clock (Input to the UUT)
70	TAP1 GND	
71	TAP1 IO1	Discrete Input/Output to the UUT
72	TAP1 GND	
73	TAP1 IO2	Discrete Input/Output to the UUT
74	TAP1 GND	
75	TAP1 IO3	Discrete Input/Output to the UUT
76	TAP1 GND	
77	Reserved	Do Not Connect
78	Reserved	Do Not Connect
79	Reserved	Do Not Connect
80	Reserved	Do Not Connect

Figure 3-1. PXIE-1149.1/4E 80-pin TAP Connectors

The following PXIE-1149.1/4E TAP connectors are connected to the target board:

TAP1	- when the target has a single TAP connector
TAP1 and **TAP2**	- when the target has 2 TAP interface connectors
TAP1, **TAP2** and **TAP3**	- when the target has 3 TAP interface connectors
TAP1, **TAP2**, **TAP3** and **TAP4**	- when the target has 4 TAP interface connectors

To connect the TAP cables to the target (UUT), follow these steps in the order as follows:

1. Verify that the target power is OFF.
2. Plug the TAP cable connector to the mating target header.
3. Now you can turn the target power ON.

ALERT !

Make sure your target board is connected to GROUND prior to powering up the target board. This assures that the target-power return flows through its power supply return (GND) signal and not through the ground wire of the PXIE. Otherwise, with a 'floating' target, if the user hot-plugs the target power cable from its external supply (such as a 'brick' type power supply), there is no guarantee that the ground will make contact with the target first, before the power does. In such case, it is possible to momentarily engage the voltage pin of the target power supply connector prior to engaging the ground (return) pin. During such action, all target current will momentarily flow through the PXIE to ground, with the resulting transients possibly resetting the PXIE-1149.1/4E unit.

Connecting the TAP Signals

The PXIE-1149.1/4E contains four 20-pin TAP connectors. The signal pins are user-definable in the ScanExpress software but it is recommended to use the default configuration. The following tables enumerate the pinout for each of the USB-1149.1/E TAP connectors for the JTAG and I2C/SPI configurations.

Pin	Signal Name	Signal Description
1	TRST*	Test Reset (Input to the UUT)
2	GND	
3	TDI	Test Data In (Input to the UUT)
4	GND	
5	TDO	Test Data Out (Output from the UUT)
6	GND	
7	TMS	Test Mode Select (Input to the UUT)
8	GND	
9	TCK	Test Clock (Input to the UUT)
10	GND	
11	IO1	Discrete Input/Output to the UUT
12	GND	
13	IO2	Discrete Input/Output to the UUT
14	GND	
15	IO3	Discrete Input/Output to the UUT
16	GND	
17	Reserved	Do Not Connect
18	Reserved	Do Not Connect
19	Reserved	Do Not Connect
20	Reserved	Do Not Connect

Table 3-1. JTAG Connector Pin Assignments (Default)

Pin	Signal Name	Signal Description
1	SDA / SCK	I2C Data / SPI Clock
2	GND	
3	SCL / MOSI	I2C Clock / SPI Serial In
4	GND	
5	MISO	SPI Serial Out
6	GND	
7	CS0*	SPI Chip Select 0
8	GND	
9	CS1*	SPI Chip Select 1
10	GND	
11	CS2*	SPI Chip Select 2
12	GND	
13	CS3*	SPI Chip Select 3
14	GND	
15	CS4*	SPI Chip Select 4
16	GND	
17	Reserved	Do Not Connect
18	Reserved	Do Not Connect
19	Reserved	Do Not Connect
20	Reserved	Do Not Connect

Table 3-2. I2C/SPI Connector Pin Assignments (Default)

Chapter 4: Using the PXIE-1149.1/4E with ScanExpress

Hardware Setup

You must configure the PXIE-1149.1/4E controller in a ScanExpress application before the application can use it. This chapter uses ScanExpress Runner as an example to illustrate the initial configuration process.

Using PXIE-1149.1/4E with ScanExpress Tools

The PXIE-1149.1/4E unit is compatible with ScanExpress Runner, ScanExpress Debugger, and ScanExpress Programmer. The following steps are provided for ScanExpress Runner. Selecting the module in ScanExpress Debugger or ScanExpress Programmer is done in a similar fashion.

1. Make sure that PXIE-1149.1/4E controller is installed into the PXI peripheral slot.
2. Invoke the ScanExpress Runner application.
3. Click the **Setup** menu item and then select the **Controller** entry to display the Controller Configuration screen shown in Figure 4-1.

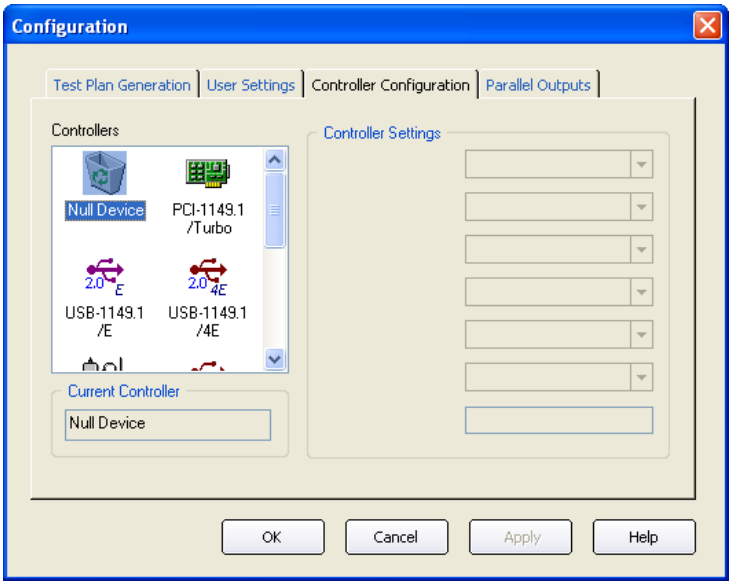


Figure 4-1. Controller Configuration Screen

4. Select the PXIE-1149.1/4E controller from the icons on the left. Adjust the controller settings to the desired values.
5. After you have made your selections, click on the **Apply** button to test and save the settings. When the program saves the settings successfully, it displays the controller in the Current Controller box. If ScanExpress Runner cannot find the controller, it displays an error dialog.
6. Once ScanExpress Runner finds the PXIE-1149.1/4E controller, it displays a screen similar to Figure 4-2.

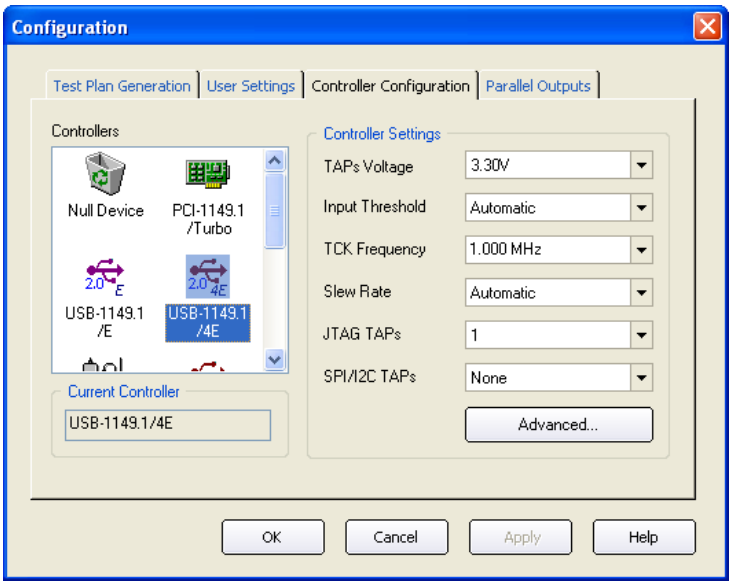


Figure 4-2. PXIE-1149.1/4E Setup Screen

Chapter 5:
Third Party Application Interface

ScanExpress Runner provides a general purpose, third-party application interface that includes specifying the correct controller and settings. This section clarifies the requirements related to the PXIE-1149.1/4E unit. Refer to the ScanExpress Runner User's Manual for further information.

Using the PXIE-1149.1/4E with the ScanExpress Runner Command-line

You can invoke ScanExpress Runner with special command line parameters to execute a Test Step file, provide test results and diagnostic messages in a log file (if you have the ScanExpress Runner ADO), and then terminate. The following table shows the controller identifiers and associated parameters. Consult the ScanExpress Runner User's Manual for more detail.

The PXIE-1149.1/4E controller uses 20 parameters. The parameters are described in the table below.

Controller keyword: **USB-1149.1/4E**

Position	Parameter	Value	Setting
1	TAPs Voltage	1 2 … 41 42 43	1.25 V 1.30 V … (0.05 volts per step) 3.25 V 3.30 V Use advanced voltage settings in position 9 through 12
2	Input Threshold	1 2 3 … 31 32 33	Automatic 0.50 V 0.55 V … (0.05 volts per step) 1.95 V 2.00 V Use advanced input threshold settings in position 13 through 16

Table 5-1. PXIE-1149.1/4E Controller Parameters

Position	Parameter	Value	Setting
3	Clock Frequency	26 … 86 87 … 114 115 … 133	75 MHz … (1 MHz increment) 15 MHz 14.5 MHz … (0.5 MHz increment) 1 MHz .950 MHz … (0.05 MHz increment) .050 MHz
4	Slew Rate	1 2 3	Automatic Slow slew rate Normal slew rate
5	JTAG TAPs Configuration	1 2 3 4 5 6 7	Use TAP1 for JTAG scanning Use TAP2 for JTAG scanning Use TAP3 for JTAG scanning Use TAP4 for JTAG scanning Use TAPs 1 and 2 in series for JTAG scanning Use TAPs 1, 2, and 3 in series for JTAG scanning Use TAPs 1, 2, 3, and 4 in series for JTAG scanning
6	SPI/I2C TAPs Default Configuration	1 2 3 4 5	Use None for direct programming Use TAP1 for direct programming Use TAP2 for direct programming Use TAP3 for direct programming Use TAP4 for direct programming
7	Delay Compensation	1 2 3 4 5 6 7 8	Automatic No Delay 0.5 Clock Delay 1.0 Clock Delay 1.5 Clock Delay 2.0 Clock Delay 2.5 Clock Delay 3.0 Clock Delay
8	TAPs Off State	1 2	Active (JTAG signals are driven when tests are not running) Tri-State

Table 5-1. PXIE-1149.1/4E Controller Parameters (continued)

Position	Parameter	Value	Setting
9	TAP1 Voltage	1 2 … 41 42	1.25 V 1.30 V … (0.05 V per step) 3.25 V 3.30 V
10	TAP2 Voltage	1 2 … 41 42	1.25 V 1.30 V … (0.05 V per step) 3.25 V 3.30 V
11	TAP3 Voltage	1 2 … 41 42	1.25 V 1.30 V … (0.05 V per step) 3.25 V 3.30 V
12	TAP4 Voltage	1 2 … 41 42	1.25 V 1.30 V … (0.05 V per step) 3.25 V 3.30 V
13	TAP1 Input Threshold	1 2 3 … 31 32	Automatic 0.50 V 0.55 V … (0.05 volts per step) 1.95 V 2.00 V
14	TAP2 Input Threshold	1 2 3 … 31 32	Automatic 0.50 V 0.55 V … (0.05 volts per step) 1.95 V 2.00 V

Table 5-1. PXIE-1149.1/4E Controller Parameters (continued)

Position	Parameter	Value	Setting
15	TAP3 Input Threshold	1 2 3 … 31 32	Automatic 0.50 V 0.55 V … (0.05 volts per step) 1.95 V 2.00 V
16	TAP4 Input Threshold	1 2 3 … 31 32	Automatic 0.50 V 0.55 V … (0.05 volts per step) 1.95 V 2.00 V
17	TA1 Pinout Configuration	0 324508639 355965919 … 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* … (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
18	TA2 Pinout Configuration	0 324508639 355965919 … 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* … (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
19	TA3 Pinout Configuration	0 324508639 355965919 … 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* … (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*

Table 5-1. PXIE-1149.1/4E Controller Parameters (continued)

Position	Parameter	Value	Setting
19	TA3 Pinout Configuration	0 324508639 355965919 … 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* … (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*
20	TA4 Pinout Configuration	0 324508639 355965919 … 4256789809	Standard pinout configuration* (0x13579BDF): Standard pinout configuration* (0x15379BDF): Custom pinout configuration* … (Custom pinout configurations. See the *NOTE below) (0xFDB97531): Custom pinout configuration*

Table 5-1. PXIE-1149.1/4E Controller Parameters (continued)

Example:

To select a PXIE-1149.1/4E controller card with all TAP voltages of 3.30 V, automatic thresholds, TCK frequency of 1 MHz, automatic slew rate, TAP1 for JTAG, TAP2 for SPI, automatic delay compensation, tri-state the JTAG signal (when test is finished), and standard pinouts for all four TAPs, use the following "controller specification" string:

```
USB-1149.1/4E,42,1,114,1,1,3,1,2,42,42,42,42,1,1,1,1,0,0,0,0,
```

*NOTE: The pinout configuration value in decimal format represents the encoded pin numbers for the JTAG, SPI, or I2C signals. Each digit of the value in hex format corresponds to the pin number of the signals as shown in the table below.

Hex Digits	1st	2nd	3rd	4th	5th	6th	7th	8th
JTAG	TRST	TDI	TDO	TMS	TCK	IO1	IO2	IO3
SPI	SCK	MOSI	MISO	CS0	CS1	CS2	CS3	CS4
I2C	SDA	SCL	-	-	-	-	-	-

For example, the standard pinout configuration for JTAG is:

[Signal:Pin#] = [TRST:1] [TDI:3] [TDO:5] [TMS:7] [TCK:9] [IO1:11] [IO2:13] [IO3:15]

This would be represented as:

0x13579BDF (324508639 in decimal format)

As another example, the custom pinout configuration of

[Signal:Pin#] = [TRST:1] [TDI:**5**] [TDO:**7**] [TMS:**9**] [TCK:**3**] [IO1:11] [IO2:13] [IO3:15]

would be represented as:

0x15793BDF (360266719 in decimal format)

If an invalid number is used, the configuration will be set to the standard pinouts, by default. Therefore, if you want to use the standard pinout configuration, you may just use the value '0' instead of '324508639'.

Appendix A: Recommended Target Connectors

10-pin TAP Connector

The Boundary-Scan TAP is a well-defined IEEE-1149.1-compatible electrical interface between boundary-scan test equipment and the boundary-scan compatible devices on the user's target board. Boundary-scan based test equipment, such as the Corelis ScanExpress family of products, utilize a single TAP to interface to the UUT. This section explains how to implement a TAP connector that is compatible with most standard test equipment.

The UUT TAP contains 5 signals: TCK, TMS, TDO, TDI and optionally TRST*. It also contains ground signal(s). Corelis recommends the standard TAP connector shown in Figure A-1, which is widely regarded as the industry standard. Note that each signal is terminated with a resistor (discussed below) in order to improve noise immunity.

The connector on the user's target should have a standard flat cable compatible pinout to match the TAP connector described in **Error! Reference source not found.**. Figure A-1 shows the top view of the basic target 10-pin connector header (0.100 × 0.100 in. spacing):

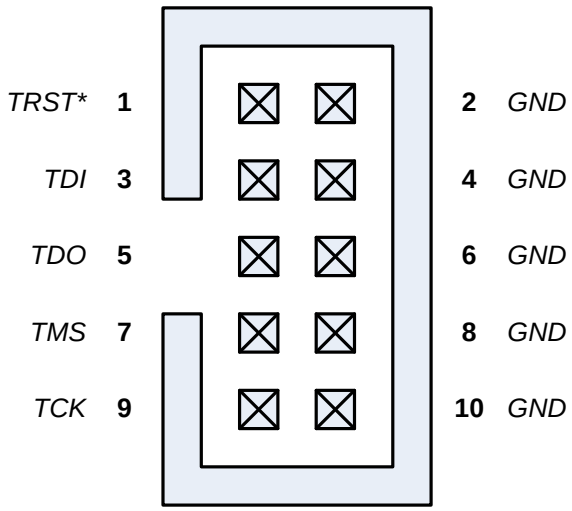


Figure A-1. Standard TAP connector (top view)

Table A-1 describes the 10 pin TAP connector signals and Corelis recommended values of terminating resistors:

Pin	Signal	Direction	Termination
1	TRST*	Input to the UUT	1K pull-up (or 1.5K pull-down)
2	GND		
3	TDI	Input to the UUT	1K pull-up
4	GND		
5	TDO	Output of the UUT	33 ohm series
6	GND		
7	TMS	Input to the UUT	1K pull-up
8	GND		
9	TCK	Input to the UUT	1K pull-up
10	GND		

Note: Some target boards may require a pull-down resistor on the TRST* signal to assure normal device operations when not in boundary-scan test mode.

Table A-1. Signal Description and Termination

Table **A-2** summarizes the specifications for the 10-pin TAP connector. Equivalent connectors are available from other manufacturers.

Reference	Description	Manufacturer	Part Number
10-Pin Target TAP	Straight header, 10-pin, 4-wall, with center notch	3M	3473-6610

Table A-2. Standard 10-Pin TAP Connector

Figure A-2 shows a typical schematic of the target TAP connector with the recommended termination resistors. The 1K pull-up resistors should connect to the target Vcc supply for the corresponding interface voltage (programmable on the PXIE-1149.1/4E from 1.25 to 3.3 V). Recommended resistor values are +/- 5%.

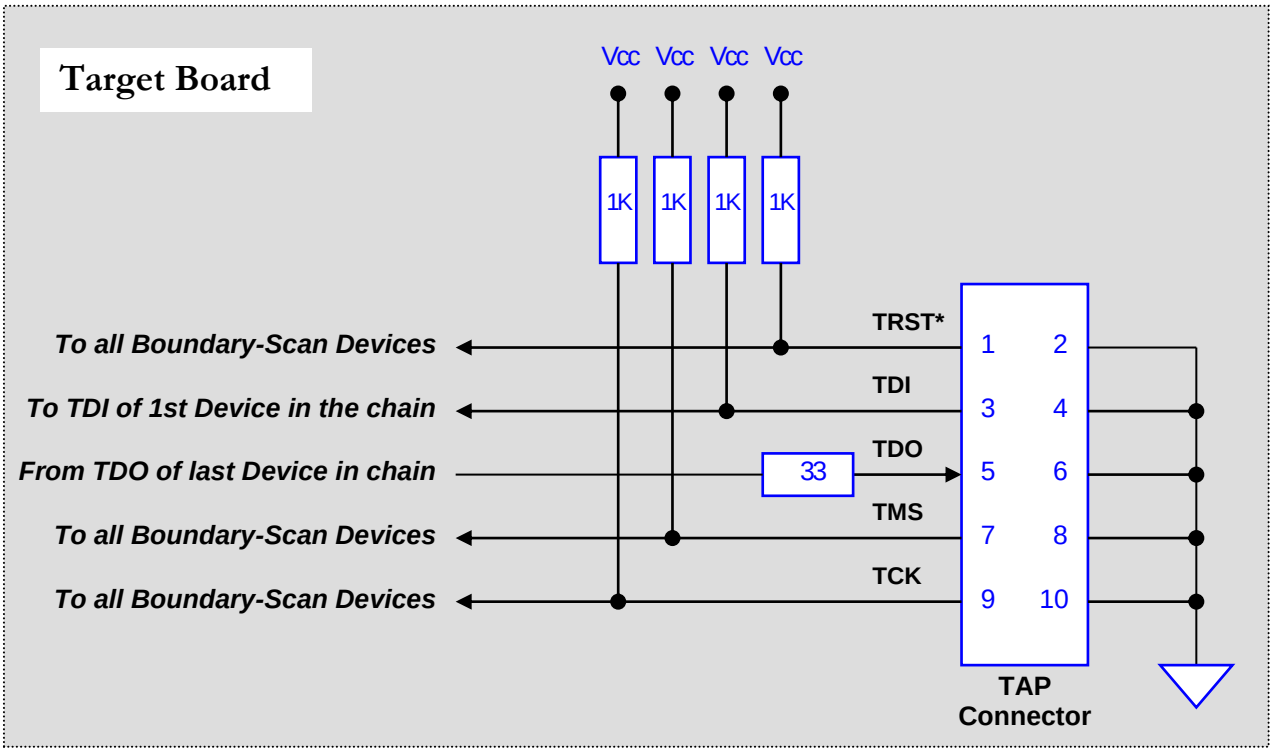


Figure A-2. TAP Connector Schematic

Flash Programming TAP Connector

To build-in support for in-circuit programming of flash or microprocessor devices, Corelis recommends including supplemental control signals in the TAP interface. The ScanExpress Programmer can use a 16-pin TAP, similar to Figure A-3, to improve programming time. This interface adds Write Strobe*, Ready/Busy*, and ground signals to the standard 5-signal interface. Terminating resistors (see Table) can improve signal quality.

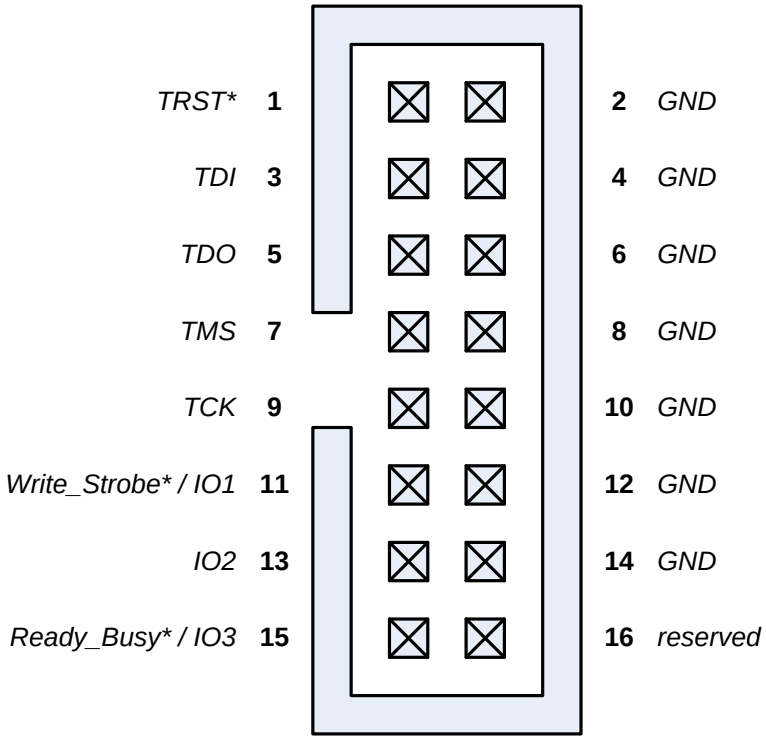


Figure A-3. Boundary-scan Flash Programming 16 Pin TAP Connector (top view)

Corelis' Flash Programming software supports the external signals Write_Strobe* and Ready/Busy*, in addition to the standard but slower scanned out/in signals approach.

The Write_Strobe* signal is active low and should be pulled up with a 1K resistor on the target board. It needs to be logically ORed with the flash Write-Enable (WE*) signal so that either the flash Write-Enable (WE*) signal or the external Write_Strobe* going low will assert the flash WE* input.

The active low Ready/Busy* signal is typically an open-collector/open-drain signal that ties directly to the same signal(s) on the Flash device(s). This enables multiple devices to drive it toward the PXIE-1149.1/4E.

Table A-3 summarizes the specifications for a 16-pin TAP connector without latch ejector. Equivalent connectors are available from other manufacturers.

Reference	Description	Manufacturer	Part Number
Flash TAP	Straight header, 16-pin, 4 wall, with center notch	3M	2516-6002UG

Table A-3. Flash Programming TAP 16 Pin Connector

Table A-4 describes the signals and Corelis recommended values for terminating resistors:

Pin	Signal	Direction	Termination
1	TRST*	Input to the UUT	1K pull-up (or 1.5K pull-down)
2	GND		
3	TDI	Input to the UUT	1K pull-up
4	GND		
5	TDO	Output from UUT	33 ohm series
6	GND		
7	TMS	Input to the UUT	1K pull-up
8	GND		
9	TCK	Input to the UUT	1K pull-up
10	GND		
11	Write_Strobe*	Input to the UUT	1K pull-up
12	GND		
13	Reserved		
14	GND		
15	Ready/Busy*	Output from UUT	1K pull-up
16	GND		

Note: Some target boards may require a pull-down resistor on the TRST* signal to assure normal device operations when not in boundary-scan test mode

Note: The target TDI signal is driven by the TDO signal of the boundary-scan controller

Note: The target TDO signal drives the boundary scan controller's TDI signal

Table A-4. Signal Description and Termination

Figure A-4 shows a typical schematic of the target TAP connector with termination resistors. The 1K pull-up resistors should connect to the target Vcc supply corresponding to the interface voltage (programmable on the PXIE-1149.1/4E from 1.25 to 3.3 V). Recommended resistor values are +/- 5%.

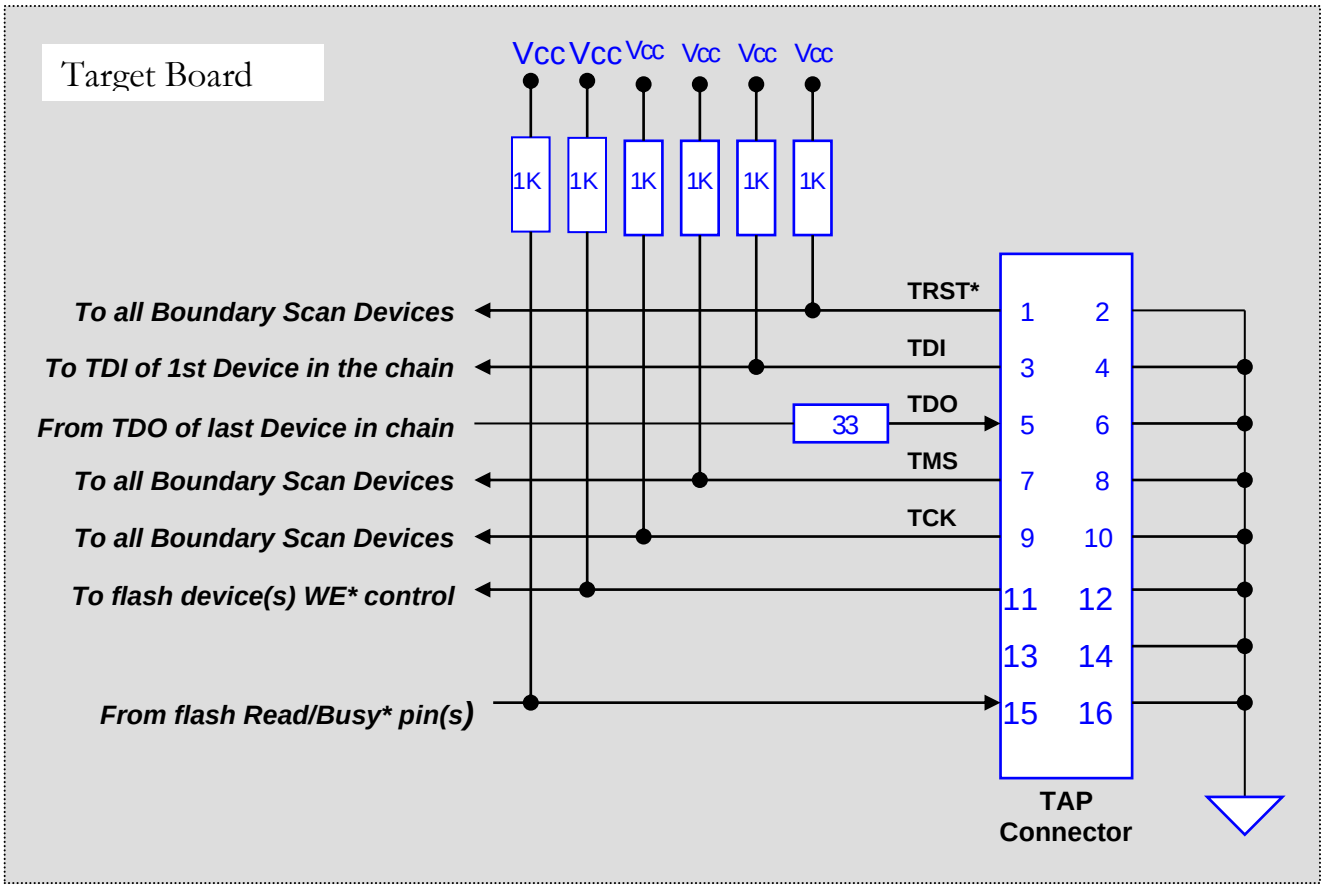


Figure A-4. Flash Programming TAP Connector Schematics

20-pin TAP Connector

To build-in support for in-circuit programming of flash or microprocessor devices, Corelis recommends including supplemental control signals in the TAP interface. The ScanExpress Programmer can use a 16-pin TAP, similar to Figure A-5, to improve programming time. This interface adds Write_Strobe*, Ready/Busy*, and ground signals to the standard 5-signal interface. Terminating resistors (see Table) can improve signal quality.

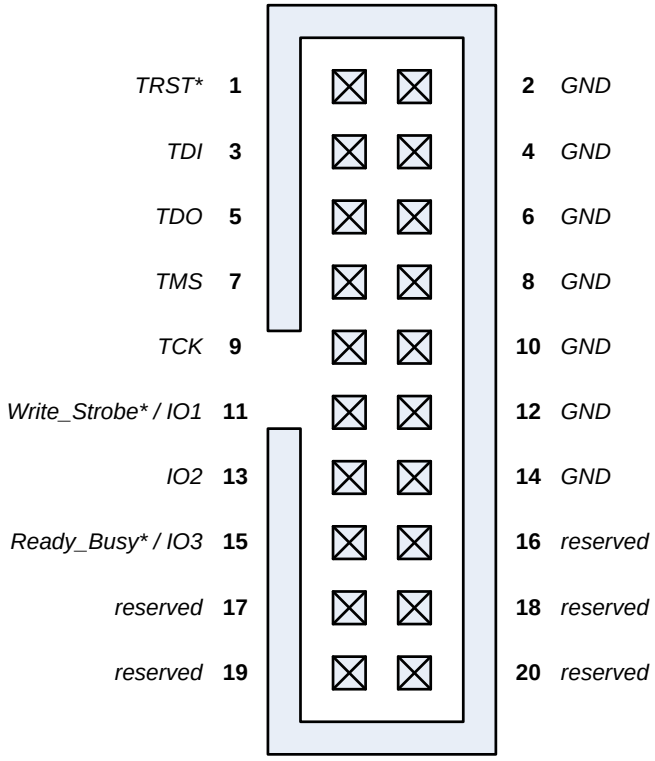


Figure A-5. Boundary-scan Flash Programming 20-Pin TAP Connector (top view)

Corelis' Flash Programming software supports the external signals Write_Strobe* and Ready/Busy*, in addition to the standard but slower scanned out/in signals approach.

The Write_Strobe* signal is active low and should be pulled up with a 1K resistor on the target board. It needs to be logically ORed with the flash Write-Enable (WE*) signal so that either the flash Write-Enable (WE*) signal or the external Write_Strobe* going low will assert the flash WE* input.

The active low Ready/Busy* signal is typically an open-collector/open-drain signal that ties directly to the same signal(s) on the Flash device(s). This enables multiple devices to drive it toward the PXIE-1149.1/4E.

Table A-5 summarizes the specifications for a 20-pin TAP connector without latch ejector. Equivalent connectors are available from other manufacturers.

Reference	Description	Manufacturer	Part Number
Flash TAP	Straight header, 20-pin, 4 wall, with center notch	3M	2520-6002UG

Table A-5. Flash Programming TAP 20-Pin Connector

Table A-6 describes the signals and Corelis recommended values of terminating resistors:

Pin	Signal	Direction	Termination
1	TRST*	Input to the UUT	1K pull-up (or 1.5K pull-down)
2	GND		
3	TDI	Input to the UUT	1K pull-up
4	GND		
5	TDO	Output from UUT	33 ohm series
6	GND		
7	TMS	Input to the UUT	1K pull-up
8	GND		
9	TCK	Input to the UUT	1K pull-up
10	GND		
11	Write_Strobe* /GPIO1	Input to the UUT	1K pull-up
12	GND		
13	GPIO2	Input to the UUT	1K pull-up
14	GND		
15	Ready_Busy* / GPIO3	Output from the UUT	1K pull-up
16	GND		
17	reserved		
18	reserved		
19	reserved		
20	reserved		

Note: Some target boards may require a pull-down resistor on the TRST* signal to assure normal device operations when not in boundary-scan test mode

Note: The target TDI signal is driven by the TDO signal of the boundary-scan controller

Note: The target TDO signal drives the boundary scan controller's TDI signal

Table A-6. Signal Description and Termination

Figure A-6 shows a typical schematic of the target TAP connector with termination resistors. The 1K pull-up resistors should connect to the target Vcc supply corresponding to the interface voltage (programmable on the PXIE-1149.1/4E from 1.25 to 3.3 V). Recommended resistor values are +/- 5%.

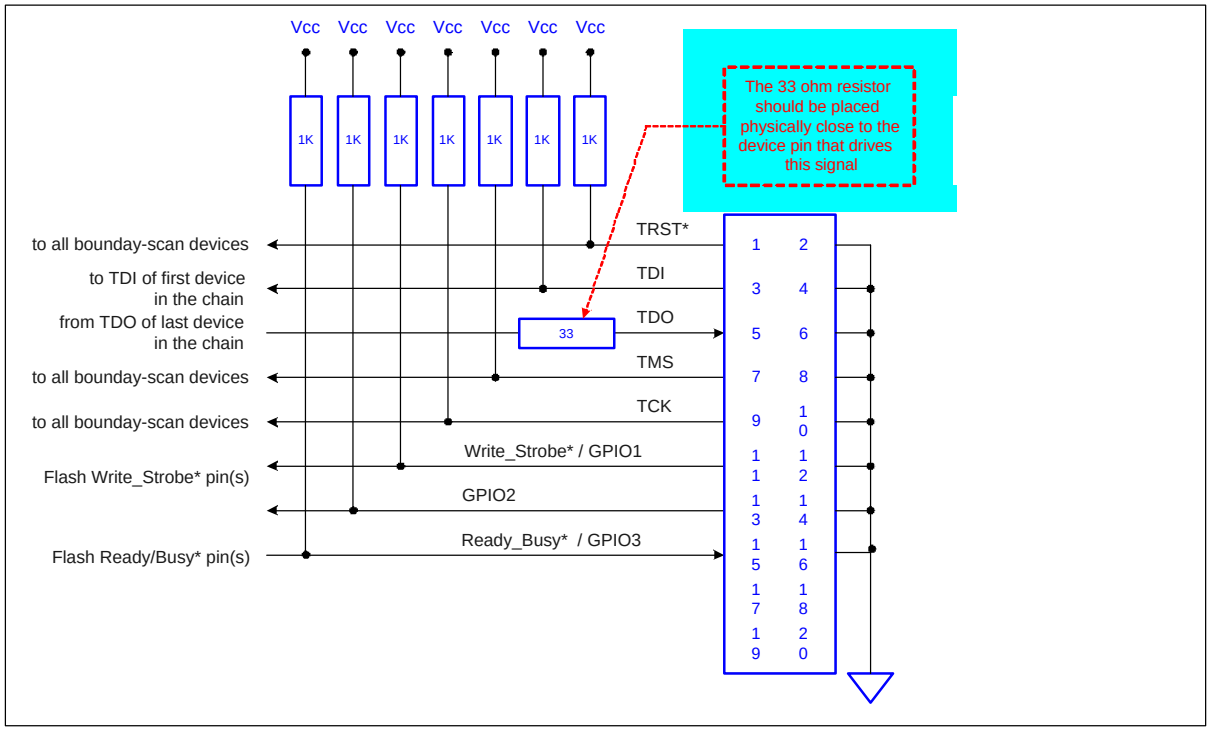


Figure A-6. 20-pin TAP Connector Schematic for JTAG

Appendix B:
Self-Test Utility Software

The PXIE-1149.1/4E has a self-test utility that can be used to test the unit and make sure that it is fully functional. Logic at the TAP connectors can read back data shifted out on TMS and TDO synchronously with the TCK. Using these signal paths, a host can test the TAP signals all the way to the connectors, verifying the overall functionality of the system.

Self-Test

The self-test utility is provided as an off-line confidence test only. Under normal circumstances, there is no need to run the self-test utility software. However, if there is a possibility that the product is damaged, un the self-test on the PXIE-1149.1/4E module. The self-test utility can be found installed in the same folder where the ScanExpress Applications (ScanExpress Runner, ScanExpress Debugger and ScanExpress Programmer) applications are also installed on your computer. Make sure to disconnect any target cables before running the test.

Using Windows Explorer, select and run the "**1149_4E_test.exe**" file. A small pop-up should appear. Click on **Test** to run the self-test.

The program should respond with a "PASSED" result on the screen shown in Figure B-1.

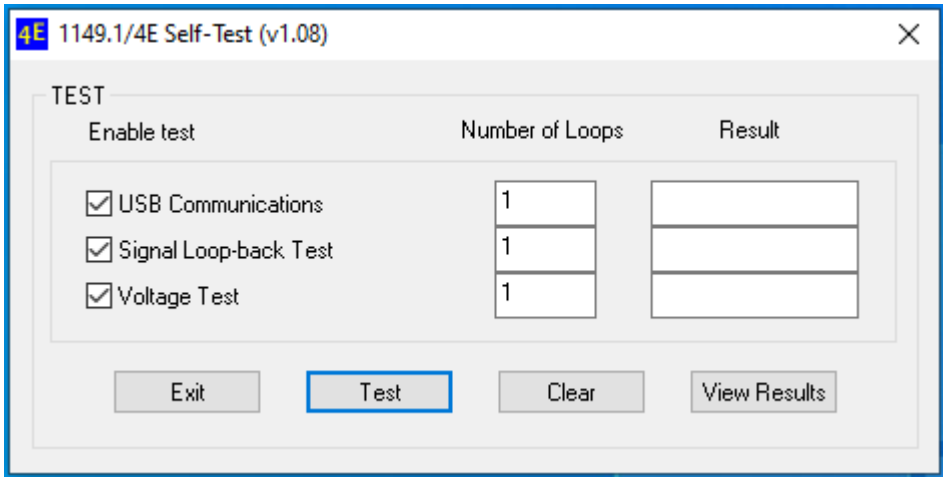


Figure B-1. Self-Test Results for the PXIE-1149.1/4E