CORELIS

SCANIO™-280LV

SCANIO™-280LV Boundary-Scan Based Digital Tester

User's Manual

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Document Part Number: 70146 REV D

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PRINTING HISTORY

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software code may be printed before the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1, July 1999
Edition 2, November 2001
Edition 3, June 2002
Edition 4, February 2011

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Chapter 1
Product Overview

Introduction

The SCANIO™-280LV Digital Tester module provides a low cost alternative to traditional stimulus response digital testing. Through the use of boundary-scan technology, the SCANIO™-280LV module provides a total of 288 fully bidirectional test channels with virtually unlimited memory depth per pin.

The module uses boundary-scan gate arrays to add control and visibility to connectors, traces, and logic that are otherwise untestable using boundary-scan techniques. The SCANIO™-280, combined with a boundary-scan controller such as the Corelis PCI-1149.1, PC-1149.1/100F, or Net-1149.1, operates as a traditional "bed of nails" test system except access to the stimulus-and-response I/Os is accomplished using boundary-scan technology.

Each pin can be individually configured as an input, output, or tri-state. Blocks of 144 I/O channels can be bypassed (using the boundary-scan bypass command), thus reducing the number of channels to fit the number of UUT I/O's. Reducing the number of I/O channels reduces test times which can be important in time-critical test applications.

Features of the SCANIO™-280LV

The SCANIO™-280LV is built around two fully boundary-scan compliant chips and supports 288 individually controllable digital I/O. The TAP and digital I/O are 5V tolerant and their interface voltage can be configured to interface with 2.5V, 3.3V or 5.0V systems. The SCANIO™-280LV can be daisy chained on a single TAP to other SCANIO™-280LVs or targets.

Figure 1-1 shows a block diagram of the SCANIO™-280LV.

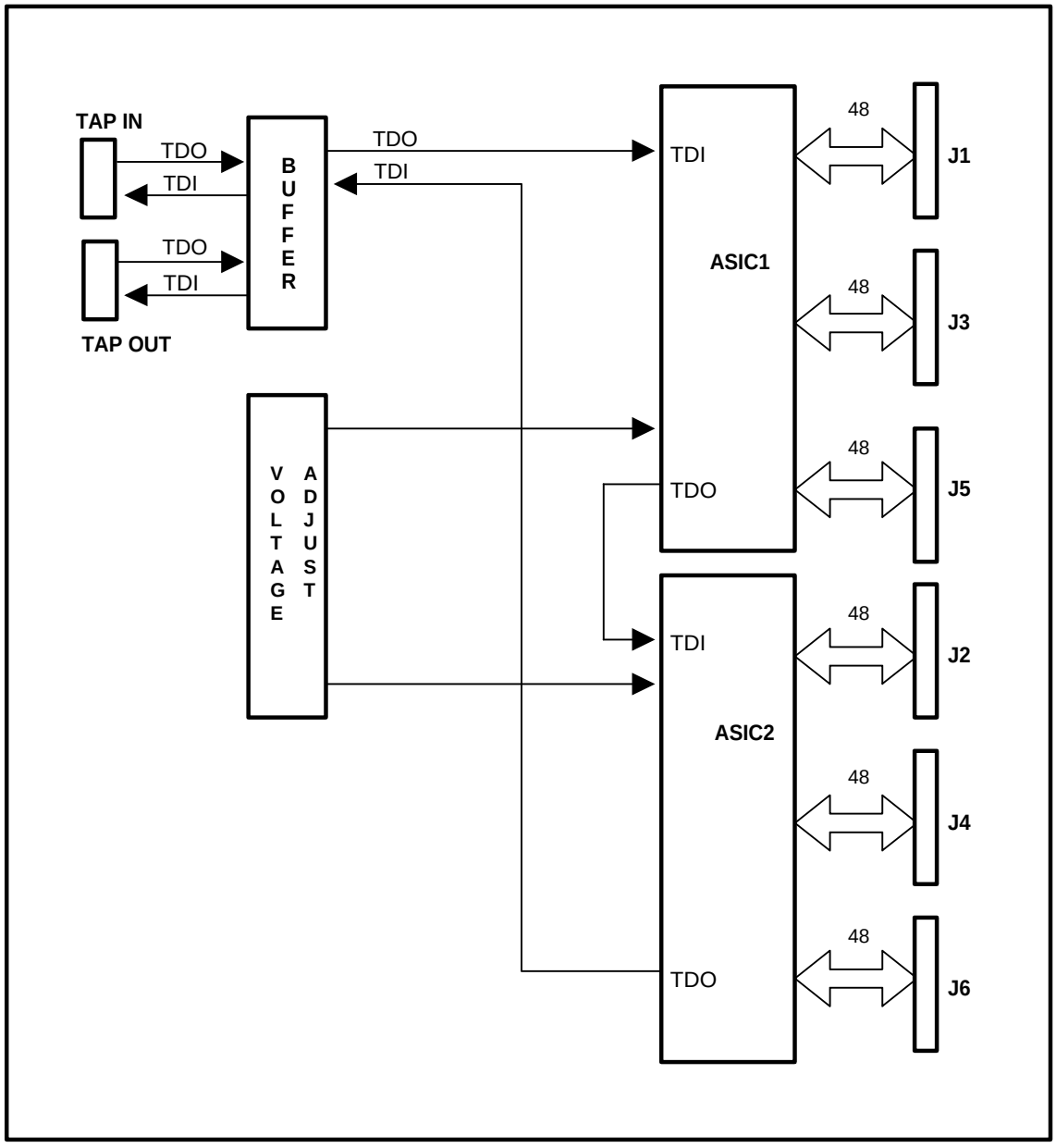

Figure 1-1. SCANIO™-280LV Block Diagram

288 Individually Controlled I/O Signals

The SCANIO™-280LV contains two ASICS each with 144 individually controlled I/O signals. Each I/O has a boundary-scan input cell, output cell and control cell associated with it. Each pin can individually be set to read only, write only or read and write simultaneously.

Adjustable Voltage Interfaces

The voltage level of the I/O and TAP interfaces is controlled by the adjust rotary switch and can be set to any voltage between 2.0V and 3.4V in increments of 0.10V. The SCANIO™-280LV has been characterized at 2.5V and 3.3V and has not been tested at the other voltage levels. The I/O and TAP interfaces are 5V tolerant at all voltage levels.

Daisy Chaining the TAPs

The TAP In and a TAP Out connectors are used to daisy chain the TAPs of one or more boards. Typically, the SCANIO™-280LV is connected in series with the boundary-scan target. The SCANIO™-280LV also can be used in stand-alone mode, or several SCANIO™-280LVs can be daisy chained together along with a target.

SCANIO™-280LV Specifications

Size and Form Factor

Dimensions	9.580" x 7.453" x 0.792"

Number of Test Points

288 per module, expandable to more lines by connecting multiple modules in series

Test Point Configurations Supported

Each test point is individually programmable as input, output or bidirectional

Bypass Capability

Either of the two blocks of 144 points may be bypassed on the ASICs.

Maximum ASIC Test Clock (TCK) Frequency

Maximum TCK Frequency	10MHz

I/O and TAP Signals DC Characteristics

Symbol	Parameter	Conditions	MIN	MAX	UNIT
VCC	Adjustable Voltage	3.3V and 5V interfaces	3.0	3.4	V
VCC	Adjustable Voltage	2.5V interface	2.3	2.7	V
V_{IH} High Level Input Voltage			1.7	5.75	V
V_{IL} Low Level Input Voltage			-0.5	0.8	V
V_{OH}	3.0V VCC	I_{OH}=-8mA DC	2.4		V
		I_{OH}=-0.1mA DC	VCC-0.2		V
	2.3V VCC	I_{OH}=-100μA DC	2.1		V
		I_{OH}=-1mA DC	2.0		V
		I_{OH}=-2mA DC	1.7		V
V_{OL}	3.0V VCC	I_{OL}=8mA DC		0.45	V
		I_{OL}= 0.1mA DC		0.2	V
	2.3V VCC	I_{OL}= 100μA DC		0.2	V
		I_{OL}= 1mA DC		0.4	V
		I_{OL}= 2mA DC		0.7	V
I_I	Input leakage current	$V_I = V_{CC}$ or ground	-10	10	μA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or ground	-10	10	μA

Note: It is recommended that no more than 50% of the outputs on any of the following two I/O groups be subjected to the maximum current limits specified above at any one time:

Group1: J1, J3, J5
Group2: J2, J4, J6

I/O Connectors

JTAG Connector (TAP In)	10-pin IDC (3M part no. 3793-6302 or equivalent)
JTAG Connector (TAP Out)	10-pin IDC (3M part no. 3793-6302 or equivalent)
I/O Connectors (J1-J6)	60-pin IDC (3M part no. 3372-6302 or equivalent)

Power Requirements (From External Power Supply)

5 Volts	3.0 Amp (Maximum)

Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non condensing

Storage Environment

Temperature	-40°C to 85°C

Chapter 2
SCANIO™-280LV Installation

The SCANIO™-280LV product consists of the following components:

- SCANIO™-280LV Hardware
- 5V External Power Supply
- SCANIO™-280LV Software Disk
- SCANIO™-280LV User's Manual

Ensure all materials listed are present and free from visible damage or defects before proceeding. If anything appears to be missing or damaged, contact Corelis at the number listed on the front cover immediately.

Introduction

To ensure reliable operation of the SCANIO™-280LV, it is important that it is connected properly to both the boundary-scan tester and the unit to be tested. If the design incorporates the recommended connectors and pin assignments then all connections are made with simple 1:1 cables. Figure 2-1 shows the cable connections between the JTAG controller, the SCANIO™-280LV, and the target UUT.

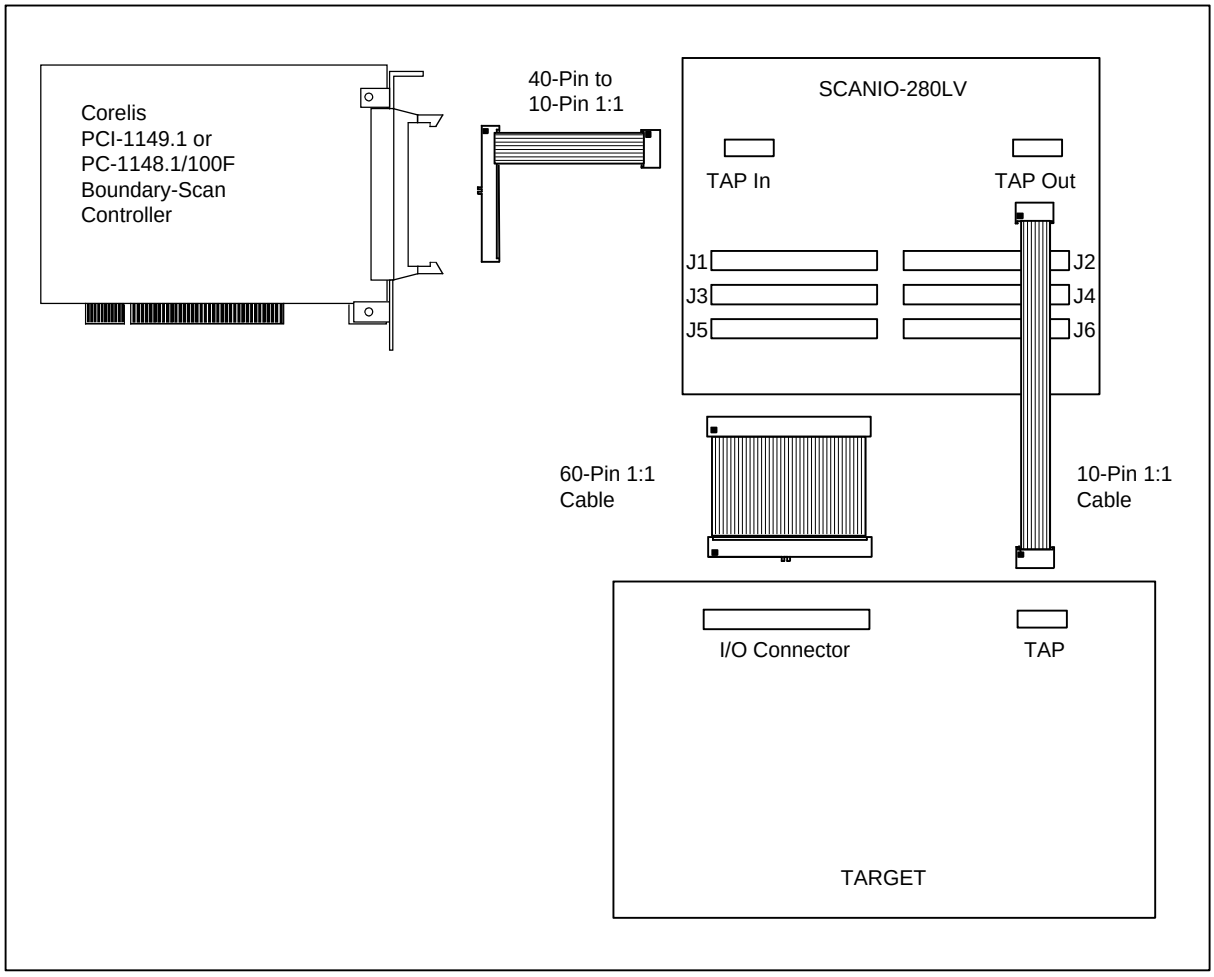

Figure 2-1. Connections Between JTAG Controller, SCANIO-280LV, and UUT

Setting the Interface Voltage

Before connecting to the boundary-scan controller or the target Unit Under Test (UUT) it is necessary to set the interface voltage. The Adjust rotary switch sets the interface voltage of the TAP and I/O pins to voltages between 2.0V and 3.4V. Use a small screwdriver to set the interface voltage. The voltage appears on the LEDs. The SCANIO™-280LV retains the set voltage interface value when powered on and off, however, it is better to check the interface voltage (by viewing the LEDs) before connecting to a target board, as an incorrect voltage setting may damage some targets.

Connecting to the JTAG Controller

The SCANIO™-280LV is connected to the JTAG controller via connector TAP In. Table 2-1 shows the pin assignment for the TAP In connector. The TAP In connector is the Corelis standard connector and can be connected to the Corelis controllers PCI-1149.1 or PC-1149.1/100F using a 40-pin to 10-pin 1:1 cable, and can be connected to the other Corelis controllers with the cable provided with them.

Pin	Signal Name	I/O	Description
1	TRST*	In	TRST*
2	GND		Ground
3	TDI	In	Test Data In
4	GND		Ground
5	TDO	Out	Test Data Out
6	GND		Ground
7	TMS	In	Test Mode Select
8	GND		Ground
9	TCK	In	Test Clock
10	GND		Ground

Table 2-1. TAP In Connection List

Target TAP Connection

Connect the target TAP to the TAP Out connector of the SCANIO™-280LV. The TAP Out connector has presence detect logic that will detect the UUT board and will include the UUT in the scan chain.

Figure 2-2 shows a diagram of this configuration. If the target system has no boundary-scan logic and no TAP, do not connect anything to TAP Out. Table 2-2 shows the connection list for the TAP Out connector.

Pin	Signal Name	I/O	Description
1	TRST_TO_UUT	Out	Test Reset to UUT scan chain
2	GND		Ground
3	TDO_TO_UUT	Out	Test Data Out to UUT scan chain
4	GND		Ground
5	TDI_FROM_UUT	In	Test Data In from UUT scan chain
6	GND		Ground
7	TMS_TO_UUT	Out	Test Mode Select to UUT scan chain
8	GND		Ground
9	TCK_TO_UUT	Out	Test Clock to UUT scan chain
10	GND		Ground

Table 2-2. TAP Out Connection List

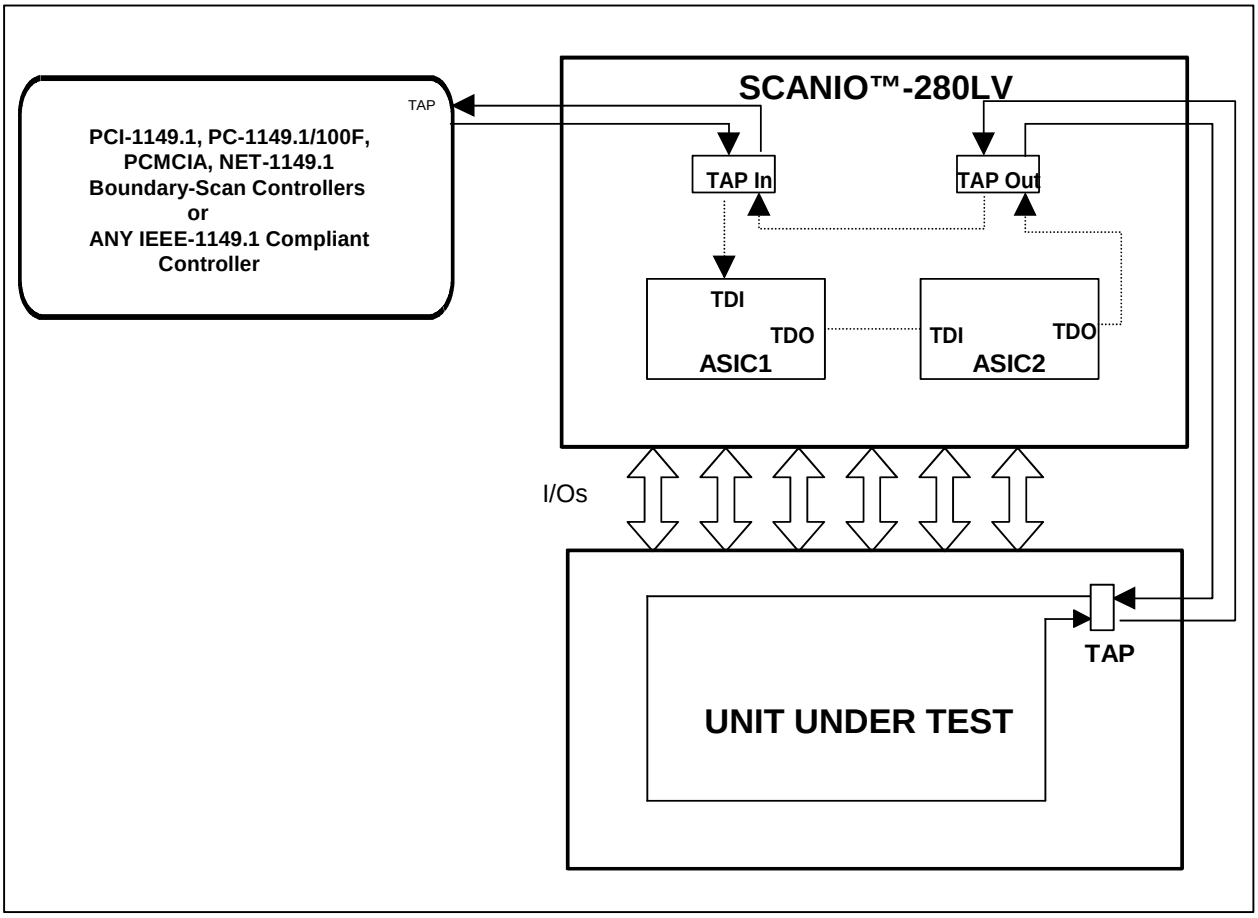

Figure 2-2. TAP Connection Between SCANIO™-280LV and UUT

Target TAP Design

The TAP contains 5 signals: TCK, TMS, TDO, TDI and optionally TRST*. It also contains ground signal(s). The Corelis recommended standard TAP connector is shown in Figure 2-3 and is widely regarded as the industry standard. Note that each signal is terminated with resistor in order to minimize signal cross-talk in the interface cable and maximize noise immunity.

The connector on the user's target should have the standard flat cable compatible pinout. Below is the top view of the target 10-pin connector header (0.100" x 0.100" spacing):

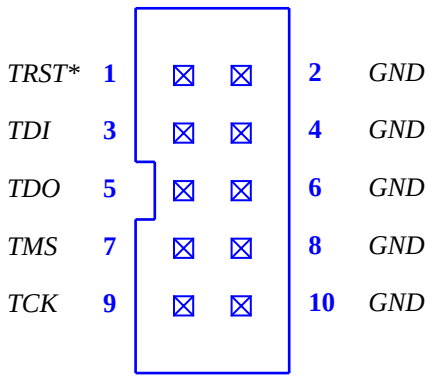

Figure 2-3. Standard TAP connector (top view)

The following are two 3M brand part numbers for the above connector. Both are 0.100" x 0.100" headers, one with and one without latch/ejector. Note that there are many other manufacturers who would have similar parts as well:

3M Part Number	*Description*
30310-6002HB	Straight header, 10 pin, 4 wall, with center notch
3793-5602UG	Latch/Ejector Straight header, 10 pin, 4 wall, with notch

Target TAP Schematics

The typical schematics of the target TAP connector and the recommended termination resistors are shown in Figure 2-4. The 1K pull-up resistors can be connected to any Vcc supply with nominal voltage between 2.5V to 5.0V. Recommended resistor values are +/- 5%.

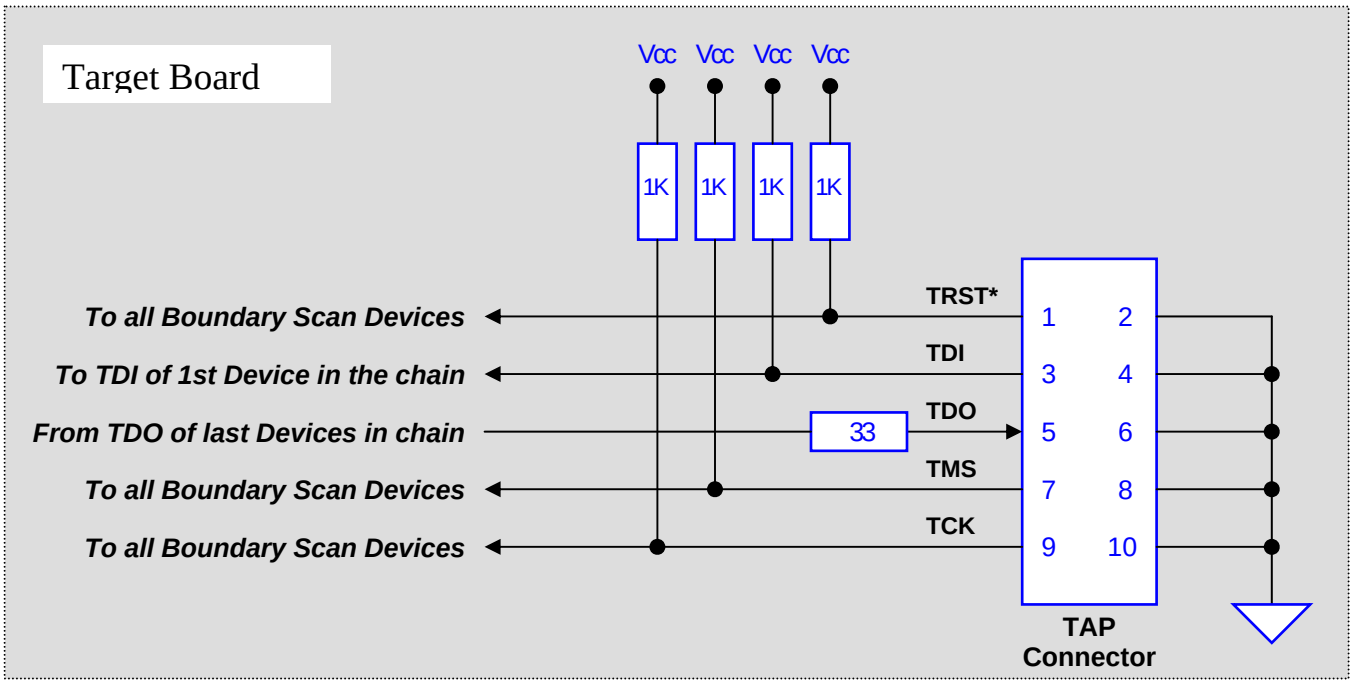

Figure 2-4. TAP Connector Schematics

Daisy Chaining the SCANIO™-280LV

The TAP Out port can be used to daisy chain multiple SCANIO™-280LV modules together to form a high pin count digital test system. A straight ten contact socket connector to socket connector flat cable can be used to connect adjacent SCANIO™-280LV modules. Connect the TAP Out from the first SCANIO™-280LV module to the TAP In on the second module. Repeat this until all modules are daisy chained. Connect the UUT to the TAP Out of the last SCANIO™-280LV. Figure 2-5 show the TAP connections for two daisy chained SCANIO™-280LV modules and a target UUT.

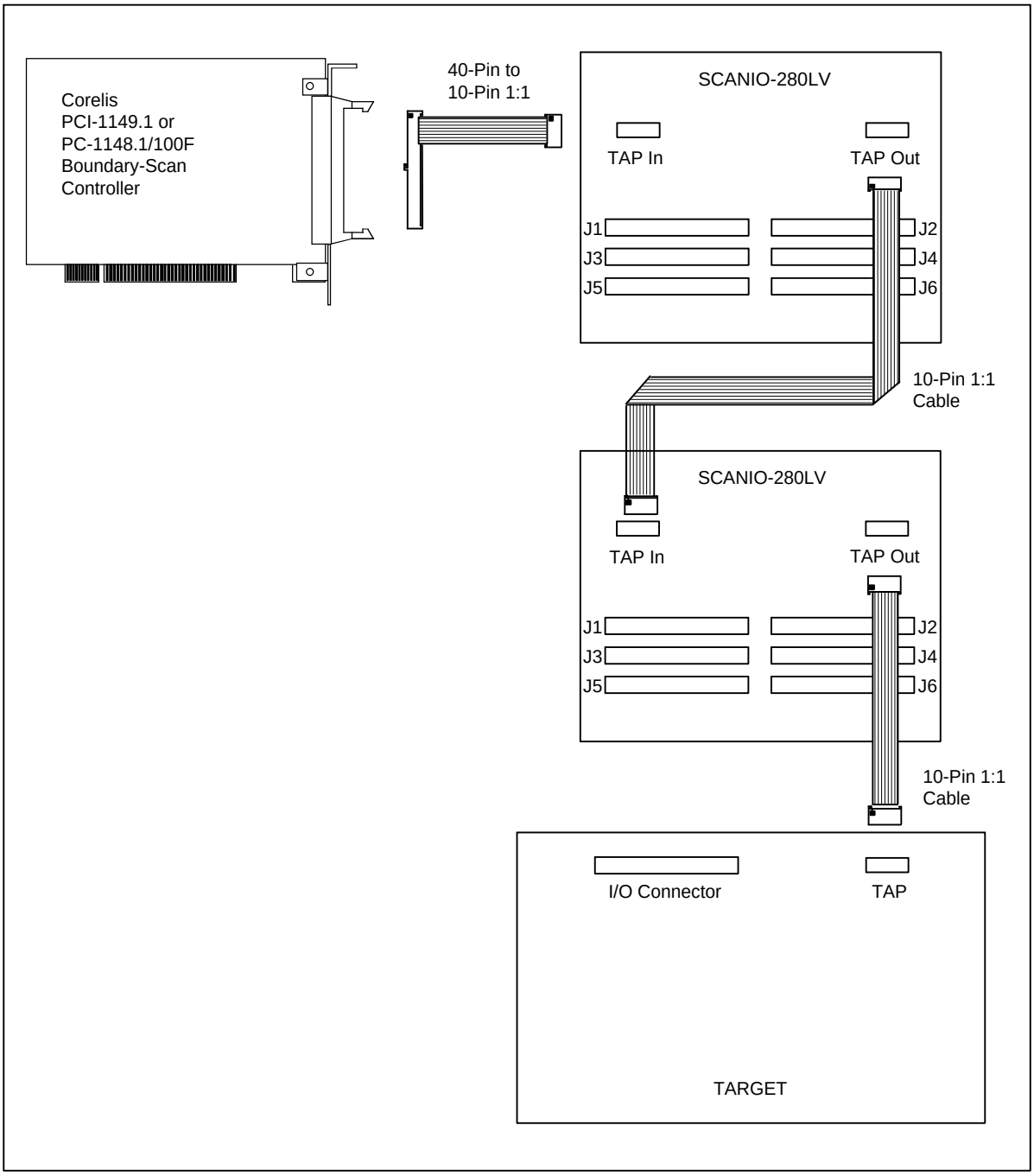

Figure 2-5. TAP Connection for Two Daisy Chained SCANIO-280LVs and a UUT

Digital I/O Test Connection

Each SCANIO™-280LV contains six 60-pin connectors which provide the digital I/O channels used for testing. Each of these 280 channels can be independently programmed as input, output or tri-state (high impedance). To create a test system, these test connectors need to be connected to the unit under test using a set of ribbon cables. Figure 2-6 shows the way that the connectors are numbered. To assist in the building of these cables Table 2-3 through Table 2-8 show the pin assignments for connectors J1 to J6.

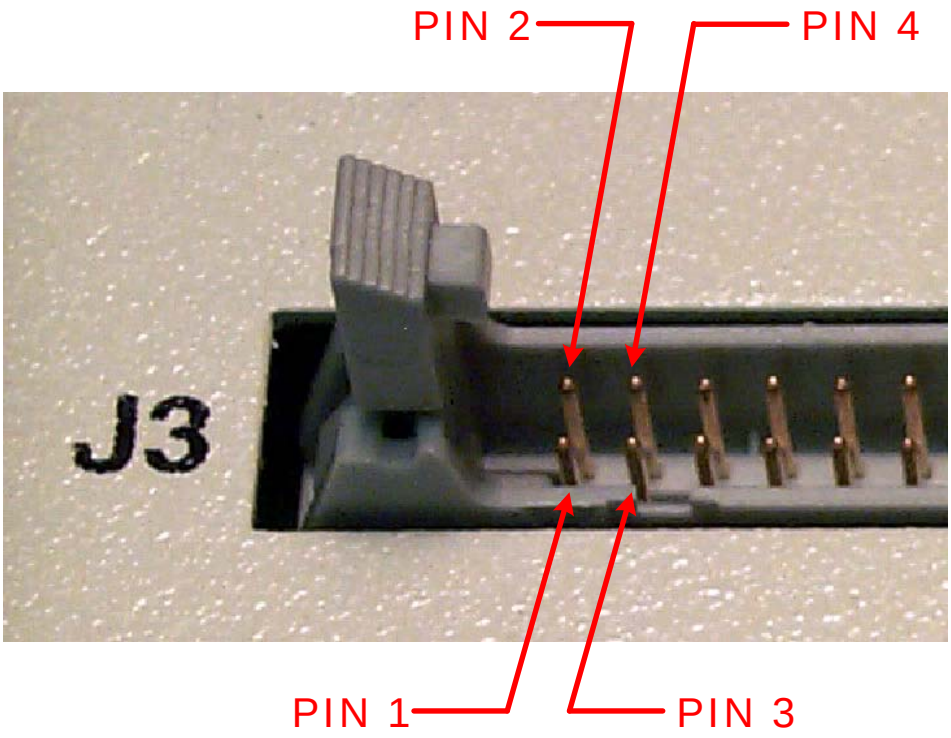

Figure 2-6. 60-pin Connector Pin Numbering

PIN	Signal	ASIC.Pin	PIN	Signal	ASIC.Pin
1	J1_1	ASIC1.101	2	J1_2	ASIC1.102
3	J1_3	ASIC1.108	4	J1_4	ASIC1.109
5	GND		6	J1_6	ASIC1.110
7	J1_7	ASIC1.111	8	J1_8	ASIC1.112
9	J1_9	ASIC1.113	10	GND	
11	J1_11	ASIC1.114	12	J1_12	ASIC1.115
13	J1_13	ASIC1.117	14	J1_14	ASIC1.118
15	GND		16	J1_16	ASIC1.119
17	J1_17	ASIC1.120	18	J1_18	ASIC1.121
19	J1_19	ASIC1.122	20	GND	
21	J1_21	ASIC1.123	22	J1_22	ASIC1.124
23	J1_23	ASIC1.126	24	J1_24	ASIC1.128
25	GND		26	J1_26	ASIC1.129
27	J1_27	ASIC1.130	28	J1_28	ASIC1.131
29	J1_29	ASIC1.132	30	GND	
31	J1_31	ASIC1.133	32	J1_32	ASIC1.135
33	J1_33	ASIC1.136	34	J1_34	ASIC1.137
35	GND		36	J1_36	ASIC1.138
37	J1_37	ASIC1.139	38	J1_38	ASIC1.140
39	J1_39	ASIC1.141	40	GND	
41	J1_41	ASIC1.142	42	J1_42	ASIC1.144
43	J1_43	ASIC1.145	44	J1_44	ASIC1.146
45	GND		46	J1_46	ASIC1.147
47	J1_47	ASIC1.148	48	J1_48	ASIC1.149
49	J1_49	ASIC1.150	50	GND	
51	J1_51	ASIC1.151	52	J1_52	ASIC1.153
53	J1_53	ASIC1.154	54	J1_54	ASIC1.159
55	GND		56	J1_56	ASIC1.160
57	J1_57	ASIC1.161	58	J1_58	ASIC1.162
59	J1_59	ASIC1.163	60	GND	

Table 2-3. J1 Connector Pin Assignment

PIN	Signal	ASIC.Pin	PIN	Signal	ASIC.Pin
1	J2_1	ASIC2.101	2	J2_2	ASIC2.102
3	J2_3	ASIC2.108	4	J2_4	ASIC2.109
5	GND		6	J2_6	ASIC2.110
7	J2_7	ASIC2.111	8	J2_8	ASIC2.112
9	J2_9	ASIC2.113	10	GND	
11	J2_11	ASIC2.114	12	J2_12	ASIC2.115
13	J2_13	ASIC2.117	14	J2_14	ASIC2.118
15	GND		16	J2_16	ASIC2.119
17	J2_17	ASIC2.120	18	J2_18	ASIC2.121
19	J2_19	ASIC2.122	20	GND	
21	J2_21	ASIC2.123	22	J2_22	ASIC2.124
23	J2_23	ASIC2.126	24	J2_24	ASIC2.128
25	GND		26	J2_26	ASIC2.129
27	J2_27	ASIC2.130	28	J2_28	ASIC2.131
29	J2_29	ASIC2.132	30	GND	
31	J2_31	ASIC2.133	32	J2_32	ASIC2.135
33	J2_33	ASIC2.136	34	J2_34	ASIC2.137
35	GND		36	J2_36	ASIC2.138
37	J2_37	ASIC2.139	38	J2_38	ASIC2.140
39	J2_39	ASIC2.141	40	GND	
41	J2_41	ASIC2.142	42	J2_42	ASIC2.144
43	J2_43	ASIC2.145	44	J2_44	ASIC2.146
45	GND		46	J2_46	ASIC2.147
47	J2_47	ASIC2.148	48	J2_48	ASIC2.149
49	J2_49	ASIC2.150	50	GND	
51	J2_51	ASIC2.151	52	J2_52	ASIC2.153
53	J2_53	ASIC2.154	54	J2_54	ASIC2.159
55	GND		56	J2_56	ASIC2.160
57	J2_57	ASIC2.161	58	J2_58	ASIC2.162
59	J2_59	ASIC2.163	60	GND	

Table 2-4. J2 Connector Pin Assignment

PIN	Signal	ASIC.Pin	PIN	Signal	ASIC.Pin
1	J3_1	ASIC1.39	2	J3_2	ASIC1.40
3	J3_3	ASIC1.42	4	J3_4	ASIC1.43
5	GND		6	J3_6	ASIC1.44
7	J3_7	ASIC1.45	8	J3_8	ASIC1.46
9	J3_9	ASIC1.47	10	GND	
11	J3_11	ASIC1.48	12	J3_12	ASIC1.49
13	J3_13	ASIC1.55	14	J3_14	ASIC1.56
15	GND		16	J3_16	ASIC1.57
17	J3_17	ASIC1.58	18	J3_18	ASIC1.58
19	J3_19	ASIC1.60	20	GND	
21	J3_21	ASIC1.61	22	J3_22	ASIC1.62
23	J3_23	ASIC1.64	24	J3_24	ASIC1.65
25	GND		26	J3_26	ASIC1.66
27	J3_27	ASIC1.67	28	J3_28	ASIC1.68
29	J3_29	ASIC1.69	30	GND	
31	J3_31	ASIC1.70	32	J3_32	ASIC1.71
33	J3_33	ASIC1.73	34	J3_34	ASIC1.76
35	GND		36	J3_36	ASIC1.77
37	J3_37	ASIC1.78	38	J3_38	ASIC1.79
39	J3_39	ASIC1.80	40	GND	
41	J3_41	ASIC1.81	42	J3_42	ASIC1.84
43	J3_43	ASIC1.86	44	J3_44	ASIC1.67
45	GND		46	J3_46	ASIC1.88
47	J3_47	ASIC1.89	48	J3_48	ASIC1.90
49	J3_49	ASIC1.91	50	GND	
51	J3_51	ASIC1.92	52	J3_52	ASIC1.93
53	J3_53	ASIC1.95	54	J3_54	ASIC1.96
55	GND		56	J3_56	ASIC1.97
57	J3_57	ASIC1.98	58	J3_58	ASIC1.99
59	J3_59	ASIC1.100	60	GND	

Table 2-5. J3 Connector Pin Assignment

PIN	Signal	ASIC.Pin	PIN	Signal	ASIC.Pin
1	J4_1	ASIC2.39	2	J4_2	ASIC2.40
3	J4_3	ASIC2.42	4	J4_4	ASIC2.43
5	GND		6	J4_6	ASIC2.44
7	J4_7	ASIC2.45	8	J4_8	ASIC2.46
9	J4_9	ASIC2.47	10	GND	
11	J4_11	ASIC2.48	12	J4_12	ASIC2.49
13	J4_13	ASIC2.55	14	J4_14	ASIC2.56
15	GND		16	J4_16	ASIC2.57
17	J4_17	ASIC2.58	18	J4_18	ASIC2.58
19	J4_19	ASIC2.60	20	GND	
21	J4_21	ASIC2.61	22	J4_22	ASIC2.62
23	J4_23	ASIC2.64	24	J4_24	ASIC2.65
25	GND		26	J4_26	ASIC2.66
27	J4_27	ASIC2.67	28	J4_28	ASIC2.68
29	J4_29	ASIC2.69	30	GND	
31	J4_31	ASIC2.70	32	J4_32	ASIC2.71
33	J4_33	ASIC2.73	34	J4_34	ASIC2.76
35	GND		36	J4_36	ASIC2.77
37	J4_37	ASIC2.78	38	J4_38	ASIC2.79
39	J4_39	ASIC2.80	40	GND	
41	J4_41	ASIC2.81	42	J4_42	ASIC2.84
43	J4_43	ASIC2.86	44	J4_44	ASIC2.67
45	GND		46	J4_46	ASIC2.88
47	J4_47	ASIC2.89	48	J4_48	ASIC2.90
49	J4_49	ASIC2.91	50	GND	
51	J4_51	ASIC2.92	52	J4_52	ASIC2.93
53	J4_53	ASIC2.95	54	J4_54	ASIC2.96
55	GND		56	J4_56	ASIC2.97
57	J4_57	ASIC2.98	58	J4_58	ASIC2.99
59	J4_59	ASIC2.100	60	GND	

Table 2-6. J4 Connector Pin Assignment

PIN	Signal	ASIC.Pin	PIN	Signal	ASIC.Pin
1	J5_1	ASIC1.187	2	J5_2	ASIC1.188
3	J5_3	ASIC1.190	4	J5_4	ASIC1.192
5	GND		6	J5_6	ASIC1.193
7	J5_7	ASIC1.194	8	J5_8	ASIC1.195
9	J5_9	ASIC1.196	10	GND	
11	J5_11	ASIC1.197	12	J5_12	ASIC1.198
13	J5_13	ASIC1.199	14	J5_14	ASIC1.201
15	GND		16	J5_16	ASIC1.202
17	J5_17	ASIC1.203	18	J5_18	ASIC1.204
19	J5_19	ASIC1.205	20	GND	
21	J5_21	ASIC1.206	22	J5_22	ASIC1.3
23	J5_23	ASIC1.4	24	J5_24	ASIC1.6
25	GND		26	J5_26	ASIC1.7
27	J5_27	ASIC1.8	28	J5_28	ASIC1.9
29	J5_29	ASIC1.10	30	GND	
31	J5_31	ASIC1.11	32	J5_32	ASIC1.12
33	J5_33	ASIC1.13	34	J5_34	ASIC1.15
35	GND		36	J5_36	ASIC1.16
37	J5_37	ASIC1.17	38	J5_38	ASIC1.18
39	J5_39	ASIC1.19	40	GND	
41	J5_41	ASIC1.20	42	J5_42	ASIC1.21
43	J5_43	ASIC1.22	44	J5_44	ASIC1.24
45	GND		46	J5_46	ASIC1.25
47	J5_47	ASIC1.26	48	J5_48	ASIC1.27
49	J5_49	ASIC1.28	50	GND	
51	J5_51	ASIC1.29	52	J5_52	ASIC1.31
53	J5_53	ASIC1.33	54	J5_54	ASIC1.34
55	GND		56	J5_56	ASIC1.35
57	J5_57	ASIC1.36	58	J5_58	ASIC1.37
59	J5_59	ASIC1.38	60	GND	

Table 2-7. J5 Connector Pin Assignment

PIN	Signal	ASIC.Pin	PIN	Signal	ASIC.Pin
1	J6_1	ASIC2.187	2	J6_2	ASIC2.188
3	J6_3	ASIC2.190	4	J6_4	ASIC2.192
5	GND		6	J6_6	ASIC2.193
7	J6_7	ASIC2.194	8	J6_8	ASIC2.195
9	J6_9	ASIC2.196	10	GND	
11	J6_11	ASIC2.197	12	J6_12	ASIC2.198
13	J6_13	ASIC2.199	14	J6_14	ASIC2.201
15	GND		16	J6_16	ASIC2.202
17	J6_17	ASIC2.203	18	J6_18	ASIC2.204
19	J6_19	ASIC2.205	20	GND	
21	J6_21	ASIC2.206	22	J6_22	ASIC2.3
23	J6_23	ASIC2.4	24	J6_24	ASIC2.6
25	GND		26	J6_26	ASIC2.7
27	J6_27	ASIC2.8	28	J6_28	ASIC2.9
29	J6_29	ASIC2.10	30	GND	
31	J6_31	ASIC2.11	32	J6_32	ASIC2.12
33	J6_33	ASIC2.13	34	J6_34	ASIC2.15
35	GND		36	J6_36	ASIC2.16
37	J6_37	ASIC2.17	38	J6_38	ASIC2.18
39	J6_39	ASIC2.19	40	GND	
41	J6_41	ASIC2.20	42	J6_42	ASIC2.21
43	J6_43	ASIC2.22	44	J6_44	ASIC2.24
45	GND		46	J6_46	ASIC2.25
47	J6_47	ASIC2.26	48	J6_48	ASIC2.27
49	J6_49	ASIC2.28	50	GND	
51	J6_51	ASIC2.29	52	J6_52	ASIC2.31
53	J6_53	ASIC2.33	54	J6_54	ASIC2.34
55	GND		56	J6_56	ASIC2.35
57	J6_57	ASIC2.36	58	J6_58	ASIC2.37
59	J6_59	ASIC2.38	60	GND	

Table 2-8. J6 Connector Pin Assignment

Mating Connectors

Table 2-9 shows the mating connectors needed to make cables for the JTAG connector and the I/O port connectors. Table 2-10 shows the mating 40-pin TAP connector for the PCI-1149.1 and the PC-1149.1/100F.

Reference	Description	Manufacturer	Part Number
TAP In, TAP Out	10 pin .100 x .100 Wiremount Socket	3M	3473-6610
	Strain Relief	3M	3448-3010
J1-J6	60 pin .100 x .100 Wiremount Socket	3M	3334-6660
	Strain Relief	3M	3448-3060

Table 2-9. Mating Connectors for the SCANIO™-280LV

Reference	Description	Manufacturer	Part Number
P1	40 pin .100 x .100 Wiremount Socket	3M	3417-6640
	Strain Relief	3M	3448-3040

Table 2-10. Mating TAP Connector for PCI-1149.1 and PC-1149.1/100F

Chapter 3
Provided Software

What's on the Disk

The disk contains the following files:

Filename	Description
ASIC280LV.bsd	BSDL file for the SCANIO™-280LV boundary-scan components.
Scanio.edt	Netlist edit file for use with Corelis ScanPlus tools.
Scanio.net	Partial netlist shows connection of the digital I/Os of the two boundary-scan components.
Scanio.top	Boundary-scan topology file for use with Corelis ScanPlus tools. Shows the scan chain from TDI to TDO of the SCANIO™-280LV.
\Example\74bct8374	BSDL file for SN74BCT8374 boundary-scan chips on example Unit Under Test.
\Example\ASIC280LV.bsd	BSDL file for the SCANIO™-280LV boundary-scan components.
\Example\JDB.net	Telesis format netlist of example UUT.
\Example\Scanio&JDB.edt	Netlist edit file for example UUT and SCANIO™-280LV.
\Example\Scanio&JDB.top	Topology file showing scan chain for example UUT and SCANIO™-280LV.
\Example\STD_1149_1_1990	1990 IEEE 1149.1 VHDL Package
\Example\STD_1149_1_1994	1994 IEEE 1149.1 VHDL Package
\Selftest\ASIC280LV.bsd	BSDL file for the SCANIO™-280LV boundary-scan components.
\Selftest\Scanio.top	Boundary-scan topology file for use with Corelis ScanPlus tools. Shows the scan chain from TDI to TDO of the SCANIO™-280LV.
\Selftest\Scanio.net	Partial netlist shows connection of the digital I/Os of the two boundary-scan components.
\Selftest\ScanioLoopBack.edt	Netlist edit file that merges connectors J1 with J2, J3 with J4 and J5 with J6 for use with ScanPlus TPG for loopback test pattern generation.
\Selftest\Selftest_Buswire_bus.cvf	Selftest buswire test vector file. Requires Corelis ScanPlus Runner to execute test. Must connect 60 pin 1:1 cables from J1 to J2, from J3 to J4, and from J5 to J6.
\Selftest\Selftest_Interconnect_int.cvf	Selftest interconnect test vector file. Requires Corelis ScanPlus Runner to execute test. Must connect 60 pin

Filename	Description
	1:1 cables from J1 to J2, from J3 to J4, and from J5 to J6.
\Selftest\Selftest_Infrastructure_inf.cvf	Selftest infrastructure test vector file. Requires Corelis ScanPlus Runner to execute test.
\Selftest\STD_1149_1_1994	1994 IEEE 1149.1 VHDL Package

Executing Selftest with ScanPlus Runner

The SCANIO™-280LV comes with three (3) compact vector format selftest files, Selftest_Infrastructure_inf.cvf, Selftest_Interconnect_ic.cvf Selftest_Buswire_bus.cvf . In order to execute these files you need Corelis ScanPlus Runner test execution software and a Corelis Boundary-Scan controller such as the PC-1149.1/100F or PCI-1149.1 with cable. To complete all three tests three (3) sixty pin 1:1 cables are necessary to provide loopback on the digital I/O signals.

Infrastructure Test

The infrastructure test verifies that a good TAP connection is being made between the controller and the SCANIO™-280LV. It also verifies that the boundary-scan infrastructure of the two ASICs on the SCANIO™-280LV is fully functional. The infrastructure test requires a Corelis boundary-scan controller, a SCANIO™-280LV unit and a cable to connect the two. Please follow these steps:

STEP1. Connect the 5V power supply to the SCANIO™-280LV.
STEP2. Make sure no target is connected to the SCANIO™-280LV, then power it up by turning on the Power Switch.
STEP3. Set the interface voltage by using a screwdriver to rotate the adjust switch. All three selftests can be run at any voltage.
STEP4. Connect one end of the TAP cable to the boundary-scan controller and the other end to TAP In connector on the SCANIO™-280LV.
STEP5. Double click on the ScanPlus Runner Icon.
STEP6. Select *File:New Test Plan*.
STEP7. Click on the *Add* button and add Selftest_Infrastructure_inf.cvf.
STEP8. Select OK.
STEP9. Select *Set-up:Controller* then select the boundary-scan controller being used and set the frequency to 10MHz.
STEP10. Select *Run Test*. The test should run and pass. Figure 3-1 shows a passing infrastructure test.

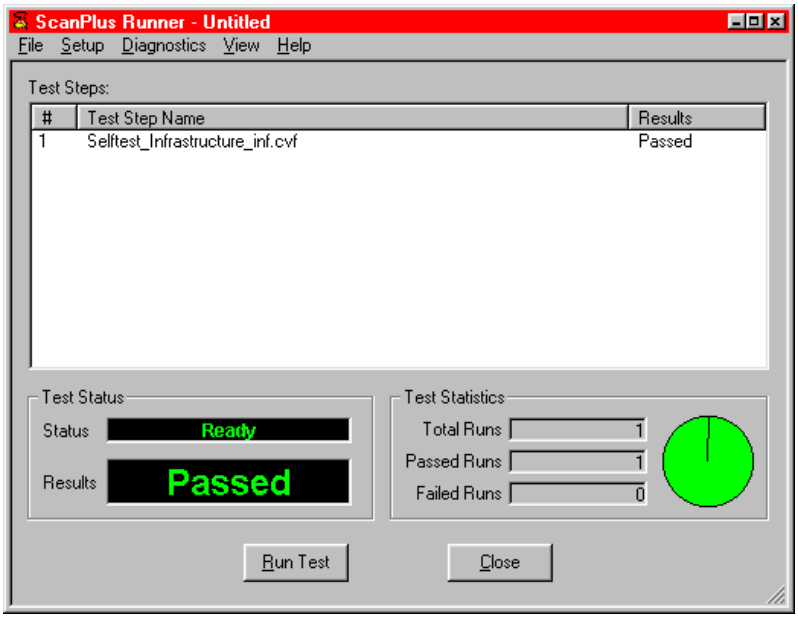

Figure 3-1. ScanPlus Runner Infrastructure Test

Interconnect and Buswire Tests

The interconnect and buswire tests verify that all 288 digital I/Os of the SCANIO™-280LV are fully functional. These tests are completed without a target attached. To test all of the I/Os, three (3) 60-pin 1:1 cables must be connected between pairs J1 and J2, J3 and J4, and J5 and J6 to establish interconnectivity between the connectors. Note that this test not only tests the SCANIO™-280LV digital I/Os but also tests the connectivity of the 60-pin 1:1 cables. If you are using 60-pin 1:1 cables to connect to your target, this is a good way to verify that the cables are good. The interconnect and buswire tests will be run in a single test plan that includes the infrastructure test. Please follow these steps:

STEP1. Connect the 5V power supply to the SCANIO™-280LV.
STEP2. Make sure no target is connected to the SCANIO™-280LV, then power it up by turning on the Power Switch.
STEP3. Set the interface voltage by using a screwdriver to rotate the adjust switch. All three selftests can be run at any voltage.
STEP4. Connect one end the TAP cable to the boundary-scan controller and the other end to TAP In Connector on the SCANIO™-280LV.
STEP5. Connect a 60-pin 1:1 cable between J1 and J2. Connect a 60-pin 1:1 cable between J3 and J4. Connect a 60-pin 1:1 cable between J5 and J6.
STEP6. Double click on the ScanPlus Runner Icon.
STEP7. Select *File:New Test Plan.*
STEP8. Click on the *Add* button and add Selftest_Infrastructure_inf.cvf, Selftest_Interconnect_ic, and Selftest_Buswire_bus.cvf in that order.
STEP9. Select OK.
STEP10. Select *Set-up:Controller* then select the boundary-scan controller being used and set the frequency to 10MHz.
STEP11. Select *Run Test.* The test should run and pass. Figure 3-2 shows the results of running these tests.

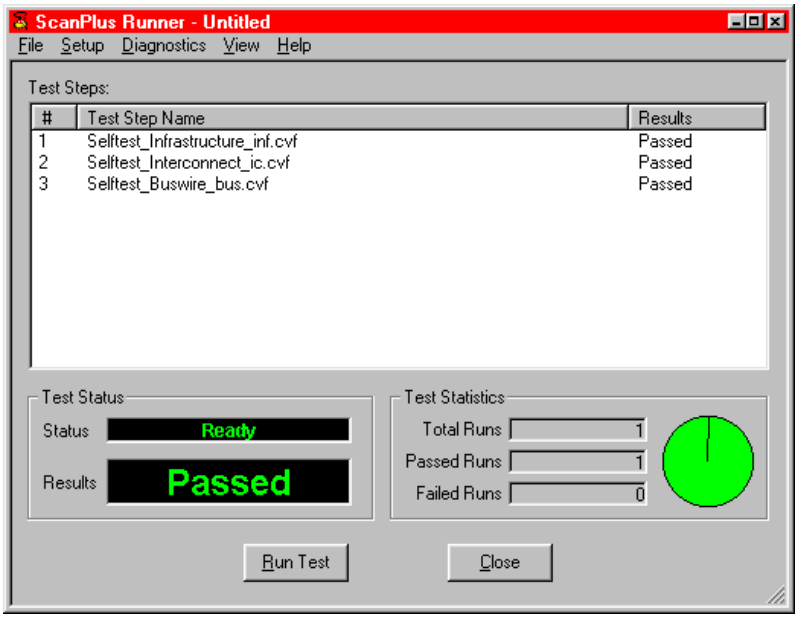

Figure 3-2. ScanPlus Runner Interconnect and Buswire Test

Using the SCANIO™-280LV Files

The SCANIO™-280LV has four files that describe its functionality: Scanio.top, Scanio.net, Scanio.edt, and Scanio.bsd. These files can also be used as inputs to the Corelis ScanPlus software.

Boundary-Scan Topology

The scan chain for the SCANIO™-280LV is described in the topology file Scanio.top shown in Figure 3-3 below. The file shows that the SCANIO™-280LV contains two boundary-scan devices in order from TDI to TDO that are referenced as ASIC1 and ASIC2. These two devices are described by BSDL file ASIC280LV.BSD and they are 208 pin PQFP devices.

When a second boundary-scan UUT is connected to the SCANIO™-280LV via the TAP Out connector, it follows the SCANIO™-280 in the boundary-scan chain. To create a new topology file describing the whole system simply add the boundary-scan components of the UUT to the Scanio.top file after ASIC2. Chapter 4 contains a complete application example.

```
!  Date:            July 12, 1999
!  Engineer:        K. May
!  Company:         Corelis Inc.
!  File:            Scanio.top
!
!  Boundary-Scan topology file for the SCANIO-280LV


CHAIN     chain1

          TDI  TDO
          TDO  TDI
          TMS  TMS
          TCK  TCK

     DEVICES
                ASIC1     "ASIC280LV.BSD"  PQFP208      NO
                ASIC2     "ASIC280LV.BSD"  PQFP208      NO
    END_DEVICES
END_CHAIN
```

Figure 3-3. Topology File Scanio.top

Boundary-Scan Description Language (BSDL)

The BSDL file for the two boundary-scan components on the SCANIO™-280LV is supplied on the software disk. ASIC280LV.bsd is used as an input file for the Corelis ScanPlus software or other Automatic Test Pattern Generator. The BSDL file can also be used as a reference for people who are writing their own boundary-scan test software. The BSDL gives description of the component pinout, signal names, boundary-scan register and boundary-scan instructions that are supported.

Netlist Edit File

The netlist edit file is used by the Corelis ScanPlus TPG tools to add digital I/O signals of the SCANIO™-280LV to the netlist of the UUT. To use this file without modification the UUT netlist must define the same signal names as the netlist edit file. Figure 3-4 shows part of the netlist edit file scanio.edt for the SCANIO™-280LV. The edit file shows the connectivity between the SCANIO™-280LV ASICs and the connectors. The naming convention for the nets is Net_*ConnectorName_PinNumber*. Line one indicates that ASIC1 pin 101 is connected to connector J1 pin 1. Chapter 4 gives a complete example on how to use the edit file and how to label nets the UUT netlist.

```
add_node ASIC1.101 NET_J1_1
add_node ASIC1.114 NET_J1_11
add_node ASIC1.115 NET_J1_12
add_node ASIC1.117 NET_J1_13
add_node ASIC1.118 NET_J1_14
add_node ASIC1.119 NET_J1_16
add_node ASIC1.120 NET_J1_17
add_node ASIC1.121 NET_J1_18
add_node ASIC1.122 NET_J1_19
add_node ASIC1.102 NET_J1_2
add_node ASIC1.123 NET_J1_21
```

Figure 3-4. Netlist Edit File Scanio.edt

Netlist

A partial Telesis format netlist, Scanio.net, is provided with the SCANIO™-280LV. The netlist shows the connectivity between the digital I/Os and the connectors on the SCANIO™-280LV. It can be used for reference or to generate a selftest for the stand-alone SCANIO™-280LV board.

Chapter 4
Application Example with ScanPlus TPG

Introduction

To assist in the application of the SCANIO™-280LV this chapter provides an example of using the SCANIO™-280LV to test the interconnects of an edge connector that is connected to boundary-scan compatible buffers and some non-boundary-scan logic. The example UUT is an actual board that is available through Corelis sales, ask for the JTAG Demo Board. Figure 4-1 shows a partial schematic for the example given in this chapter.

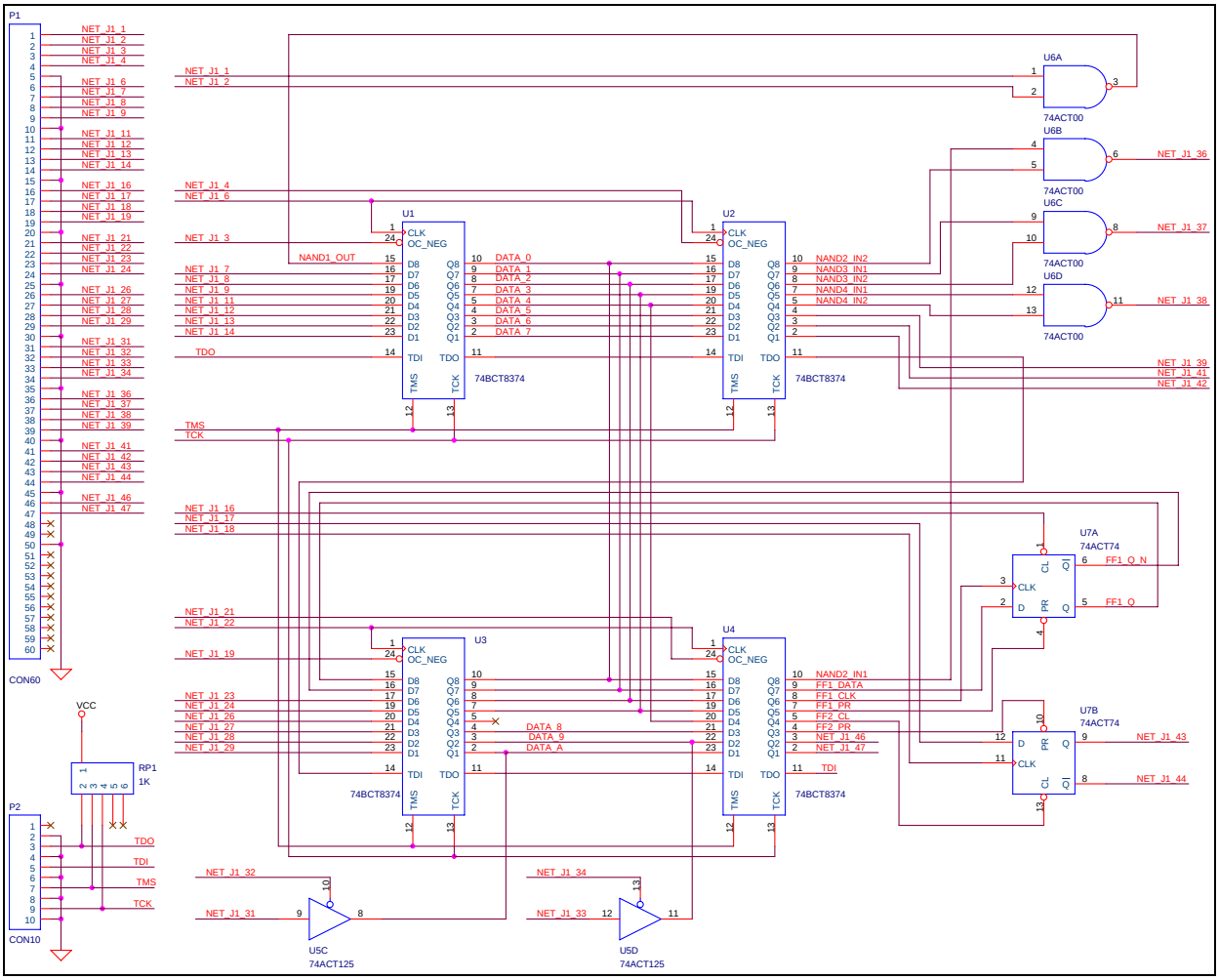

Figure 4-1. Schematic of an Example Unit Under Test

Description of the Unit Under Test

In the example shown in Figure 4-1 above only nets DATA_0-DATA_8 are fully testable. The outputs from buffers U2 and U4, the inputs to U1 and U3 which connect to either non-boundary-scan logic or the edge connector cannot be tested using boundary-scan techniques under normal circumstances since there is only one boundary-scan cell on each net. With the use of the SCANIO™-280LV the visibility of the boundary-scan chain can be expanded to include these nets.

TAP Connection and Termination

The TAP is designed to be compatible with the Corelis standard TAP and contains 4 signals: TCK, TMS, TDO and TDI. The TRST signal, pin 1 on the standard TAP connector is left unconnected since the boundary-scan chips on the target board do not contain this signal. All 5 even pins are connected to ground. Note that each signal is terminated with a 1K Ohm resistor in order to minimize signal cross-talk in the interface cable and maximize noise immunity.

SCANIO™-280LV Interface

Connector P1 on the example schematic is the interface with the SCANIO™-280LV. The net names on P1 were chosen to be the same as the net names for the J1 connector in the SCANIO™-280LV netlist, enabling easy netlist merging for Automatic Test Pattern Generation. If board space permits, it is recommended to used 60 pin 0.100" x 0.100" connectors with pinouts compatible with the SCANIO™-280LV. This allows easy connection with 1:1 cables. The following is the 3M brand part number for the above connector with latch/ejector:

3M Part Number	***Description***
3372-6302	Straight header, 60 pin, 4 wall with center notch

Sometimes the SCANIO™-280LV is used to test a particular connector on a design which is not the same connector as used on the SCANIO™-280LV. This will work too, the cable is just more complicated.

Generating Test Vectors with ScanPlus TPG

In order to generate test vectors for a system with the SCANIO™-280LV and UUT using the Corelis ScanPlus TPG it is necessary to collect/create certain files. It is advised to create a test design directory and to place all files in the same directory. A list of the various required input files is contained in this section. All files contain plain ASCII text, which can be generated or changed with any editor.

1. **Netlist file (*.net):** This file is generated by the user's CAD system and describes all of the nets and pins of a target board. In such cases where the CAD system is unable to generate a Telesis or standard Allegro compatible Netlist file, an optional utility is used to convert the standard CAD Netlist (EDIF, HDL, etc.) to the Telesis format.

2. **BSDL files (*.bsd):** The BSDL files are required for all boundary-scan components that are used in the particular design. The BSDL files are available from the original manufacturers of each particular boundary scan component. The BSDL file for the components of the

SCANIO™-280LV is ASIC280LV.bsd and can be found on the disk provided with the this product.

3. **Topology file (*.top):** This file provides information about the scan chain ordering and physical characteristics of the JTAG compatible devices on the target board. Use the provided Scanio280.top topology file as a starting point then add the devices on your target board to it. See the example below.

4. **Constraint file (*.con):** This file allows the user to set nets to specified logic levels and specify other constraints that need to be maintained when generating test vectors for the target board. This file is useful for user target boards that contain both boundary-scan and non-boundary scan components. For such cases, enable signals, chip selects, etc. are required to remain in a particular state for the duration of the test in order to prevent the non-boundary scan components from interfering with the boundary scan tests. This file is not necessary for the example presented here.

5. **Netlist Edit** file (*.edt). This file allows the user to manipulate the netlist with a series of modification instructions without having to make changes to the original netlist file. The SCANIO™-280LV comes with a netlist edit file that is used to merge the SCANIO™-280LV netlist with the target netlist.

6. **Cluster SDF** file (*.sdf). A text file that is one of two files used specifically for cluster testing. The SDF file, which conforms to the TSSI file format, specifies a list of nets which will be tested in the cluster. Cluster tests are used to test non-boundary-scan components such as U6 in example schematic in Figure 4-1. Please see your ScanPlus TPG user's manual for a more detailed description and example of cluster testing.

7. **Cluster SLF** file (*.slf). A text file that is one of two files used specifically for cluster testing. The SLF file, which conforms to the TSSI file format, provides a list of test vectors which specify patterns to be applied to various nets, and levels to sense from other nets on the cluster.

Example Topology File

To create a new topology file describing the whole system simply add the boundary-scan components of the target UUT to the provided Scanio.top file after ASIC2. Connecting the UUT to the TAP Out connector of the SCANIO™-280LV adds the UUT to the end of the scan chain. The boundary-scan components on the target board must be added to the DEVICES section of the topology file in order from TDI to TDO. Therefore, U1, U2, U3 and U4 are added to the topology file in that order as shown in Figure 4-2.

```
!  Date:            July 12, 1999
!  Engineer:        K. May
!  Company:         Corelis Inc.
!  File:       Scanio&JDB.top
!
!  Boundary-Scan topology file for the SCANIO-280 & JTAG DEMO
BOARD


CHAIN     chain1

          TDI  TDO
          TDO  TDI
          TMS  TMS
          TCK  TCK

     DEVICES
       ASIC1     "ASIC280LV.BSD"  PQFP208          NO
       ASIC2     "ASIC280LV.BSD"  PQFP208          NO
       U1        "74BCT8374"      DW_PACKAGE       NO
       U2        "74BCT8374"      DW_PACKAGE       NO
       U3        "74BCT8374"      DW_PACKAGE       NO
       U4        "74BCT8374"      DW_PACKAGE       NO

        END_DEVICES
END_CHAIN
```

Figure 4-2. Example Topology File

Using the Netlist Edit File

The netlist edit file is used for making modifications to netlists. In the case of the SCANIO™-280LV the digital I/O pins must be added to the target netlist. On SCANIO™-280LV disk a netlist edit file, Scanio.edt is provided. Because the net names for the connectors in edit file match the net names in the target schematic, the netlist edit can be used for merging the two netlists. However, the Scanio.edt file contains nets for all of the SCANIO™-280LV connectors, our design only uses pins 1-47, therefore the netlist edit file must be truncated to only contain the used nets. Each line in the netlist edit file adds a digital I/O pin to the netlist of the target board. Figure 4-3 shows the netlist edit file for the example design.

```
add_node ASIC1.101 NET_J1_1
add_node ASIC1.114 NET_J1_11
add_node ASIC1.115 NET_J1_12
add_node ASIC1.117 NET_J1_13
add_node ASIC1.118 NET_J1_14
add_node ASIC1.119 NET_J1_16
add_node ASIC1.120 NET_J1_17
add_node ASIC1.121 NET_J1_18
add_node ASIC1.122 NET_J1_19
add_node ASIC1.102 NET_J1_2
add_node ASIC1.123 NET_J1_21
add_node ASIC1.124 NET_J1_22
add_node ASIC1.126 NET_J1_23
add_node ASIC1.128 NET_J1_24
add_node ASIC1.129 NET_J1_26
add_node ASIC1.130 NET_J1_27
add_node ASIC1.131 NET_J1_28
add_node ASIC1.132 NET_J1_29
add_node ASIC1.108 NET_J1_3
add_node ASIC1.133 NET_J1_31
add_node ASIC1.135 NET_J1_32
add_node ASIC1.136 NET_J1_33
add_node ASIC1.137 NET_J1_34
add_node ASIC1.138 NET_J1_36
add_node ASIC1.139 NET_J1_37
add_node ASIC1.140 NET_J1_38
add_node ASIC1.141 NET_J1_39
add_node ASIC1.109 NET_J1_4
add_node ASIC1.142 NET_J1_41
add_node ASIC1.144 NET_J1_42
add_node ASIC1.145 NET_J1_43
add_node ASIC1.146 NET_J1_44
add_node ASIC1.147 NET_J1_46
add_node ASIC1.148 NET_J1_47
add_node ASIC1.110 NET_J1_6
add_node ASIC1.111 NET_J1_7
add_node ASIC1.112 NET_J1_8
add_node ASIC1.113 NET_J1_9
```

Figure 4-3. Netlist Edit File for Example Design

Creating Test Vectors

The files necessary for creating boundary-scan tests are on the distribution disk in the directory "Example". Copy these files over to the hard drive. Double click on ScanPlusTPG. Select *New Test Step*. Select *Interconnect*. Use the add button to add the files JDB.net, Scanio&JDB.top, and Scanio&JDB.edt. Select *Generate*. Save the test step as Scanio&JDB_Interconnect. The main window should now look like Figure 4-4. Buswire and infrastructure tests can similarly be generated by selecting the appropriate button. To fully test the example board cluster test vectors which

stimulate the non-boundary-scan components and compare the response to expected values. An explanation of this is beyond the scope of this User's Manual but can be found in the Corelis ScanPlus TPG User's Manual.

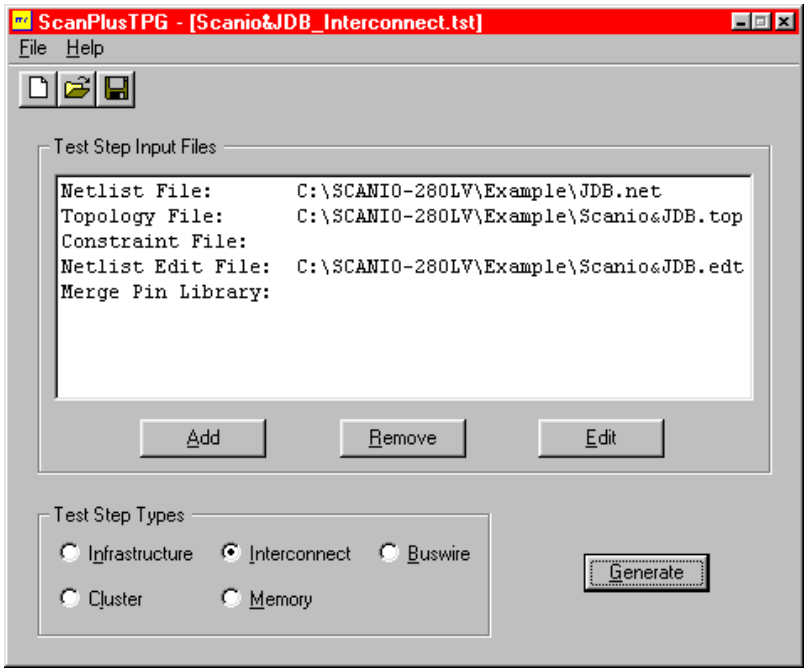

Figure 4-4. ScanPlus TPG Test Step