CORELIS

ScanIO™-300LV

ScanIO™-300LV Boundary-Scan Based Digital Tester

User's Manual

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Chapter 1
Product Overview

Introduction

The ScanIO™-300LV digital I/O module provides a low cost alternative to traditional stimulus response digital testing. Through the use of boundary-scan technology, the ScanIO-300LV module provides a total of 300 fully bidirectional test channels with virtually unlimited memory depth per pin. Multiple ScanIO-300LV units can be daisy-chained to further increase the total number of test channels.

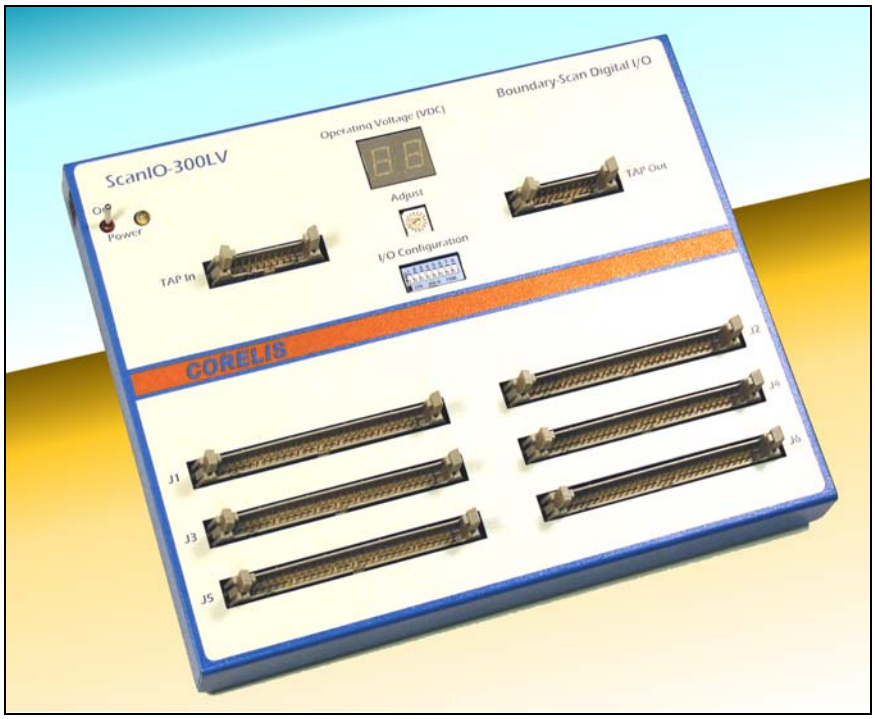

Figure 1-1. ScanIO-300LV

The module uses internal boundary-scan compatible ASICs to provide connectivity testing of non-boundary-scan compatible UUT parts such as connectors, PCB pads and test points. Using mechanical means to connect the ScanIO-300LV to the UUT connectors and/or pads allows testing of interfaces that would otherwise be untestable through boundary-scan techniques. The ScanIO-300LV, combined with a boundary-scan controller such as the Corelis PCI-1149.1/Turbo, USB-1149.1/E, or NetUSB-1149.1/E, operates as a traditional "bed of nails" test system, except access to the stimulus-and-response I/Os is accomplished using boundary-scan technology.

Six individual connectors are provided to interface to the unit under test (UUT), with each connector providing 50 test channels. Each test channel connector pin can be individually configured as an input, output, or tri-state. Note that during testing the programming and control of the test channels is automatically performed by the ScanExpress tools without any user intervention.

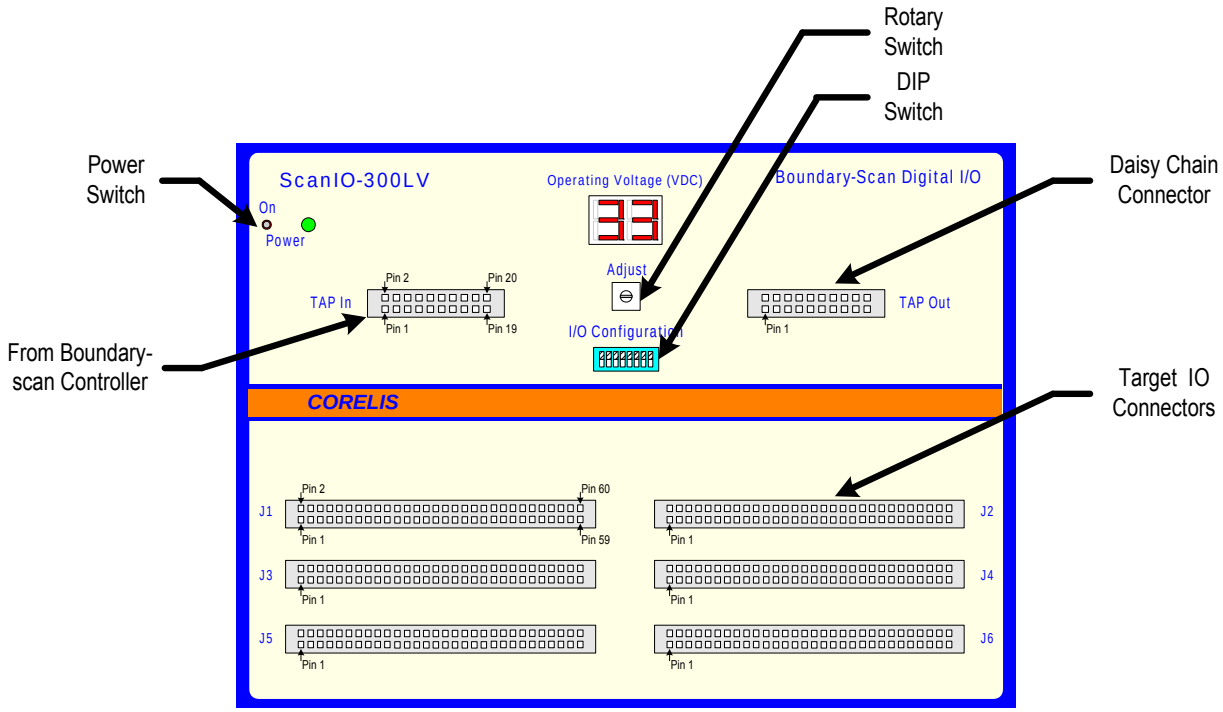

Figure 1-2. ScanIO-300LV Features

Features of the ScanIO-300LV

The ScanIO-300LV contains six (6) fully boundary-scan compliant devices and supports 300 individually controlled digital I/Os. The 5 standard boundary-scan (JTAG) test access port (TAP) signals and the 300 digital I/O signals are 3.3V tolerant and their operating voltage is programmable from 1.25V to 3.3V to match the UUT interface voltage. The ScanIO-300LV can be daisy chained to additional ScanIO-300LV units using the TAP In and TAP Out connectors. Similarly, the ScanIO-300LV can also be daisy chained to the target UUT, thereby using only a single TAP to connect the boundary-scan controller to both the ScanIO-300LV and the UUT.

Figure 1-3 shows a simplified block diagram of the ScanIO-300LV.

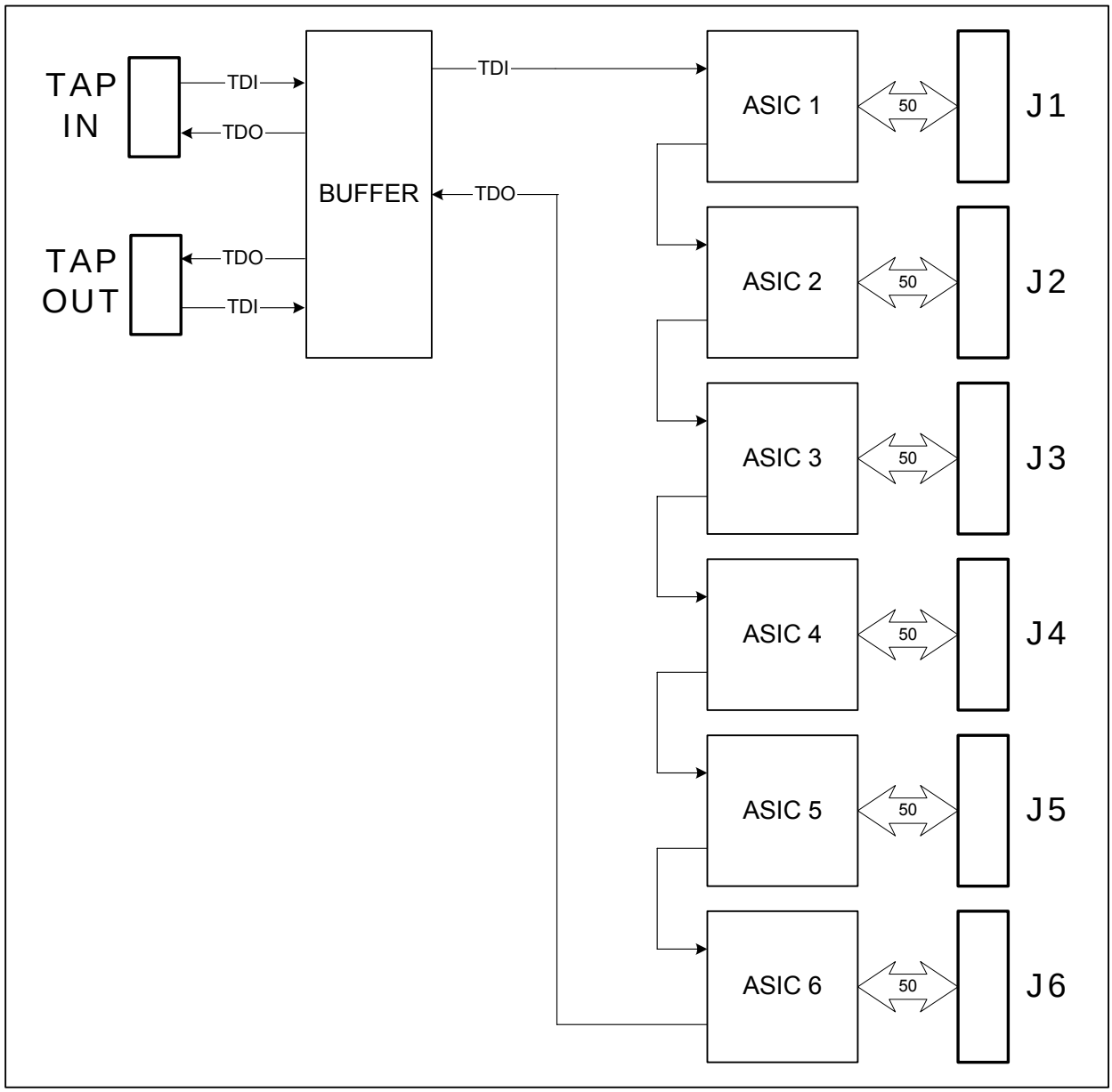

Figure 1-3. ScanIO-300LV Simplified Block Diagram

300 Individually Controlled I/O Signals

The ScanIO-300LV contains six ASICs each with 50 individually controlled I/O signals. Each ASIC is routed to its own 60 pin external connector containing the 50 I/O signals and 10 grounds. Each I/O has a boundary-scan input cell, output cell and control cell associated with it. Each pin can individually be set to read only, write only or read and write simultaneously.

Adjustable Voltage Interfaces

The voltage level of the I/O and TAP interfaces can be controlled by the adjustable rotary switch and, when using an advanced CORELIS boundary-scan controller, can also be programmed via host computer software. Contact CORELIS for a list of advanced boundary-scan controllers that provide software programmability of the ScanIO-300LV.

When using the front panel rotary switch, the user can manually set the voltage between 1.25V and 3.3V in 15 incremental steps.

LVDS Interface Configuration

The I/O type for each set of two connectors (J1/J2, J3/J4, J5/J6) can be configured to LVDS (differential) compatible signaling levels by setting the relevant front panel DIP switch(s).

Daisy Chaining the TAPs

Typically, the ScanIO-300LV is connected to the boundary-scan controller using a standard 20 pin TAP cable that connects to one of the TAP connectors of the ScanTAP intelligent pods such as the ScanTAP-4. The target UUT is connected to boundary-scan controller via different TAP cables which connect to additional TAP connector(s) of the ScanTAP pod.

Alternatively, the ScanIO-300LV and the target UUT can be connected to the boundary-scan controller using a single TAP. The TAP In and TAP Out connectors can be used to daisy chain the TAPs of one or more units. The ScanIO-300LV can be used alone, or several ScanIO-300LVs can be daisy chained together along with a target.

ScanIO-300LV Specifications

Test Channels

Number of channels	300
Direction	Input, output or bidirectional (individually programmable)

Internal ASICs

Number of ASICs	6
Test Channels per ASIC	50
Boundary-Scan BYPASS	Any of the six ASICs can be bypassed individually

TCK Clock Frequency

Maximum TCK Frequency	50MHz

Connectors

JTAG Connector (TAP IN)	20-pin shrouded header, 0.1"x0.1", 3M P/N 3428-6302
JTAG Connector (TAP OUT)	20-pin shrouded header, 0.1"x0.1", 3M P/N 3428-6302
I/O Connectors J1 - J6	60-pin shrouded header, 0.1"x0.1", 3M P/N 3372-6302

Power Requirements

5 Volts	4.0 Amp (Maximum)

Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non condensing

Storage Environment

Temperature	-40°C to 85°C

Size and Form Factor

Dimensions	9.58" ± 0.1" x 7.45" ± 0.1" x 0.79" ± 0.1"

I/O and TAP Signals DC Characteristics

Symbol	Parameter	Test Conditions	Limit Min	Limit Max	Units
V_{CC} Adjust	Adjustable Voltage		1.3	3.3	V
V_{IH}	3.3V	V_{CC} Adjust ≥ 2.5 V	2.0	3.6	V
	2.5V	1.8 < V_{CC} Adjust < 2.5 V	1.7	2.7	V
	1.8V	V_{CC} Adjust ≤ 1.8 V	65% V_{CC} Adjust	1.95	V
V_{IL}	3.3V	V_{CC} Adjust ≥ 2.5 V	-0.5	0.8	V
	2.5V	1.8 < V_{CC} Adjust < 2.5 V	-0.5	0.7	V
	1.8V	V_{CC} Adjust ≤ 1.8 V	-0.5	35% V_{CC} Adjust	V
V_{IDIFF}	LVDS Differential Input Voltage	Common mode input voltage = 1.25 V	100	-	mV
V_{ICM}	LVDS Common-mode Input Voltage	Differential input voltage = ± 350 mV	0.2	2.2	V
V_{OH}	3.3V	I_{OH} = -24 mA	2.4	-	V
	2.5V	I_{OH} = -12 mA	1.9	-	V
	1.8V	I_{OH} = -8 mA	V_{CC} Adjust - 0.4	-	V
	LVDS	100Ω across P and N signals	1.25	1.6	V
V_{OL}	3.3V	I_{OL} = 24 mA	-	0.4	V
	2.5V	I_{OL} = 12 mA	-	0.4	V
	1.8V	I_{OL} = 8 mA	-	0.4	V
	LVDS	100Ω across P and N signals	0.9	1.25	V
I_L	Input leakage current per pin	V_I = V_{CC} or Ground	-10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or Ground	-10	10	µA

Table 1-1. ScanIO-300LV Electrical Specifications

Chapter 2
ScanIO-300LV Installation

The ScanIO-300LV product consists of the following components:

- ScanIO-300LV Unit
- 5V External Power Supply
- This ScanIO-300LV User's Manual
- 20-pin JTAG Controller TAP Interface Cable
- Six generic 60-pin Target Interface Cables

Ensure all materials listed are present and free from visible damage or defects before proceeding. If anything appears to be missing or damaged, contact Corelis at the number listed on the front cover immediately.

Connecting to the Target

To ensure reliable operation of the ScanIO-300LV, it is important that it be properly connected to both the boundary-scan controller and the unit to be tested. If the design incorporates the recommended connectors and pin assignments, then all connections are made with simple 1:1 cables.

The recommended configuration is to use one of the Corelis ScanTAP family of Multiple TAP Intelligent pods such as the ScanTAP-4 to chain the TAPs. Figure 2-1 shows the cable connections between a ScanTAP-4, the ScanIO-300LV and target UUT. This supports operating the entire set of test channels and performing scan operations of the target with a single setup and automatic test plan.

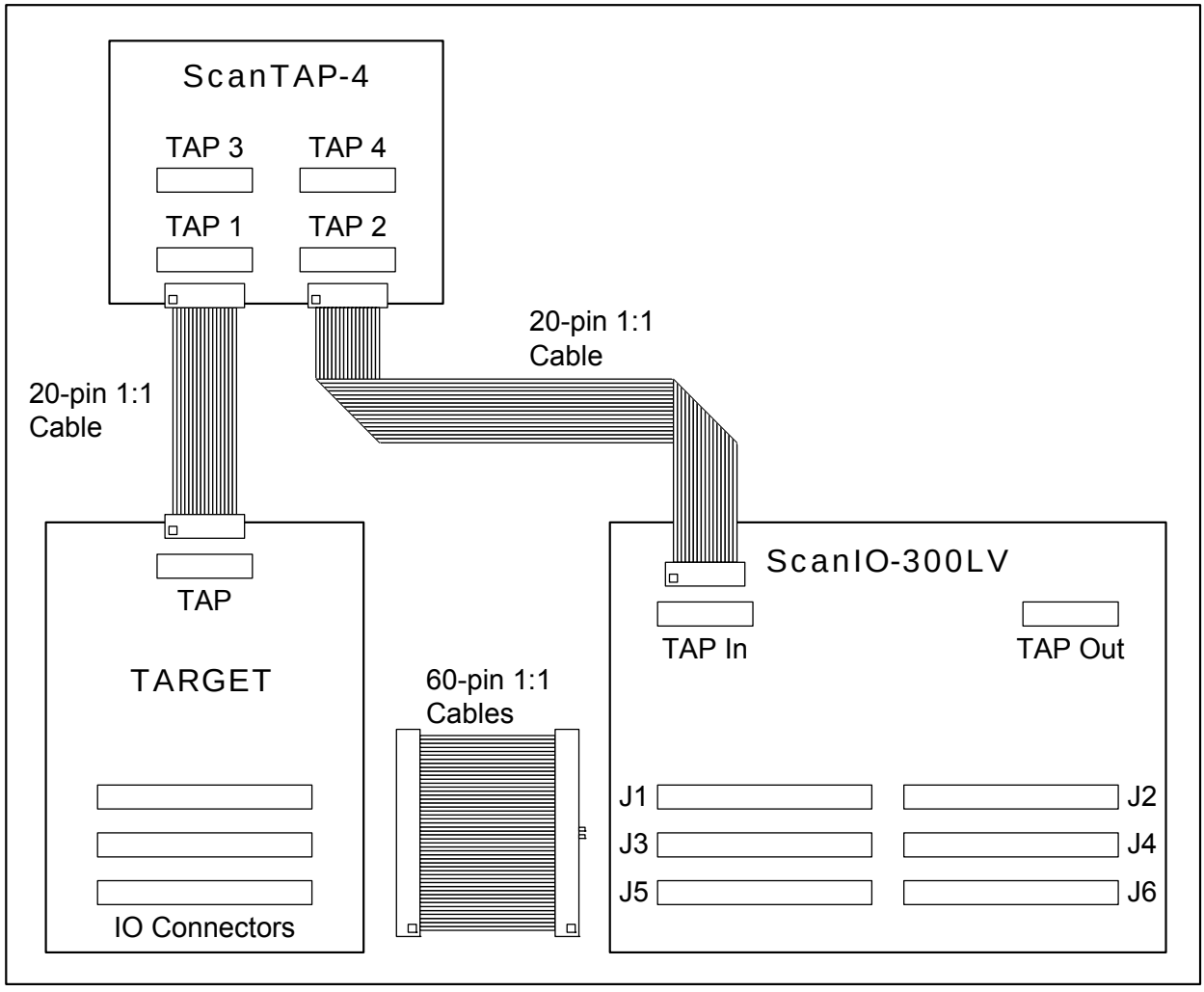

Figure 2-1. Connections Between a ScanTAP-4, ScanIO-300LV and Target

An alternative configuration uses the TAP Out connector of the ScanIO-300LV to connect to the target. This configuration should only be used when a ScanTAP pod is not available as it will lower the maximum TCK frequency. Figure 2-2 shows the cable connections between the JTAG controller, the ScanIO-300LV and the target UUT.

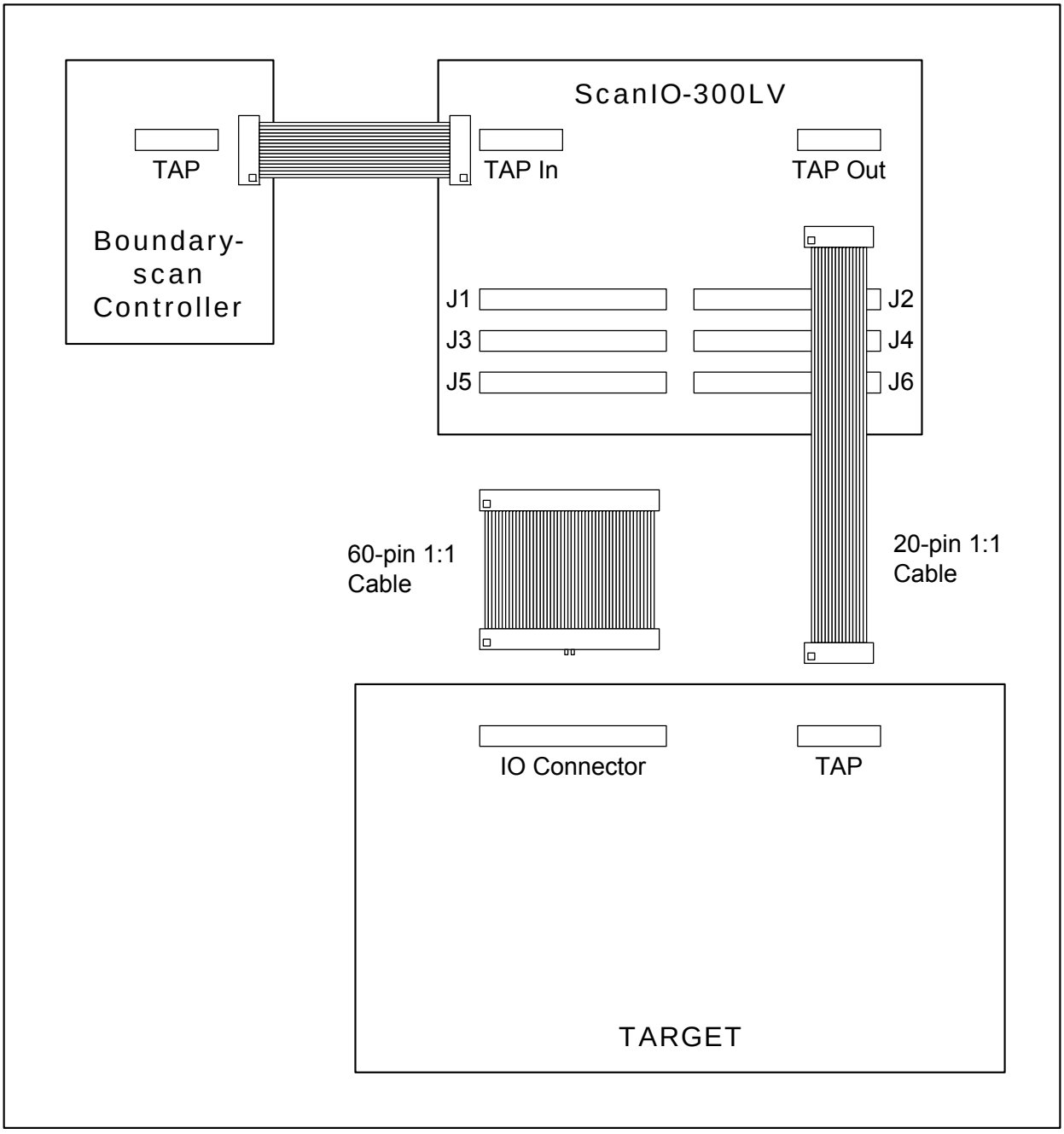

Figure 2-2. Connections Between a JTAG Controller, ScanIO-300LV and Target

Using Multiple ScanIO-300LV Units

When using multiple ScanIO-300LV units, the recommended configuration is to use a one of the Corelis ScanTAP family of Multiple TAP Intelligent pods such as the ScanTAP-4 to chain the TAPs. Figure 2-3 shows the cable connections between a ScanTAP-4, two ScanIO-300LVs and target UUT. This supports operating the entire set of test channels and performing scan operations of the target with a single setup and automatic test plan.

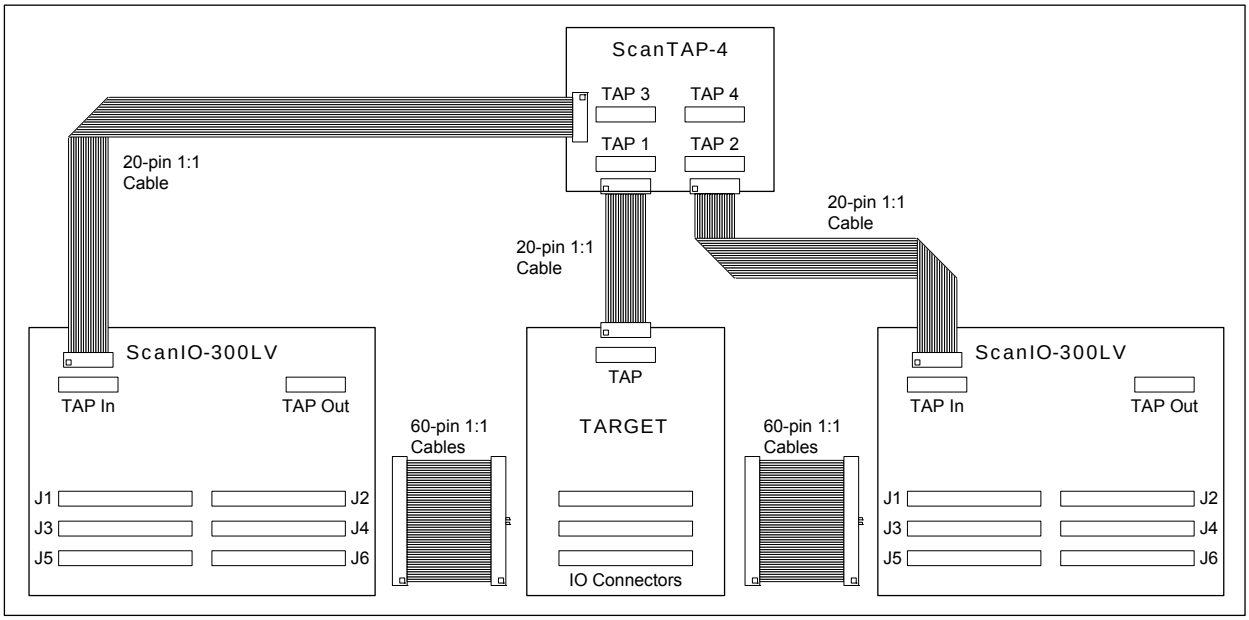

Figure 2-3. Connections Between a ScanTAP-4, Two ScanIO-300LVs and Target

The TAP Out port can be used to daisy chain multiple ScanIO-300LV modules together to form a high pin count digital test system. This configuration should only be used when a ScanTAP pod is not available as it will lower the maximum TCK frequency. A straight 20-pin flat cable can be used to connect adjacent ScanIO-300LV modules. Connect the TAP Out from the first ScanIO-300LV module to the TAP In on the second module. Repeat this until all modules are daisy chained. Connect the UUT to the TAP Out of the last ScanIO-300LV. Figure 2-4 shows the TAP connections for two daisy chained ScanIO-300LV modules and a target UUT.

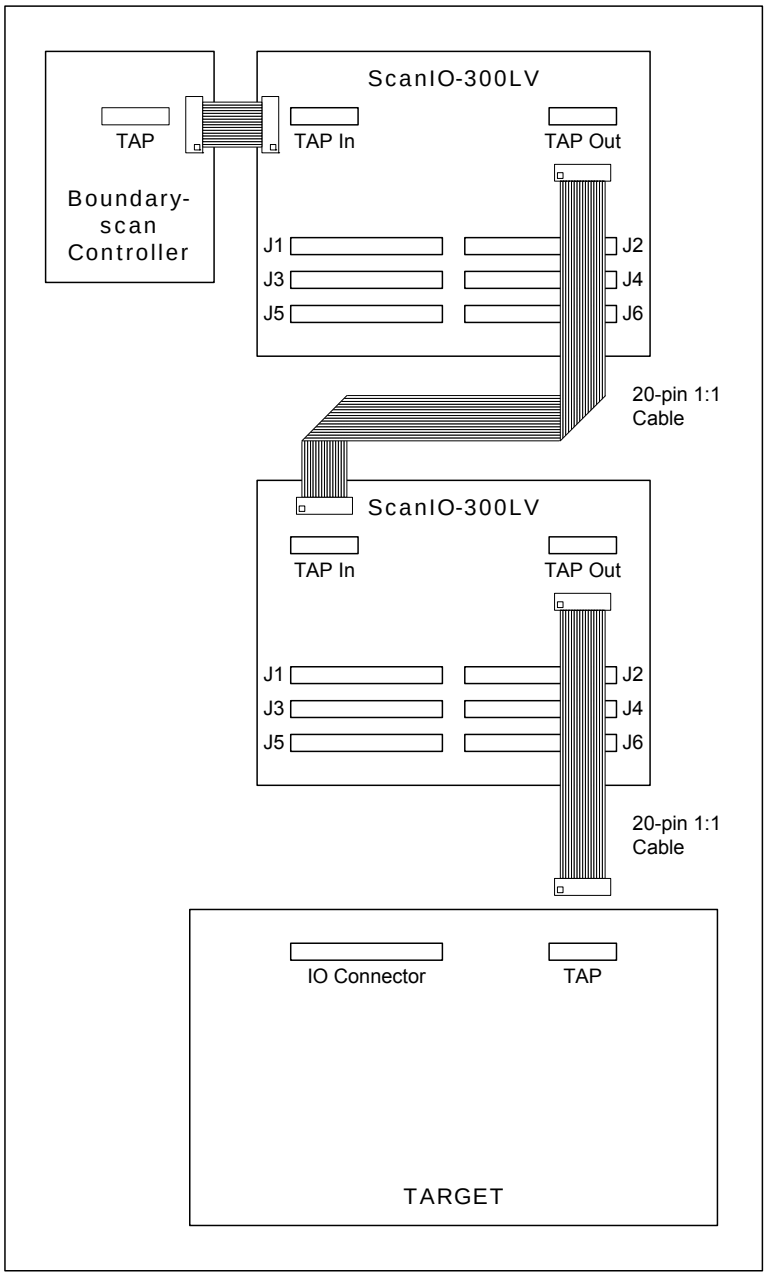

Figure 2-4. TAP Connection for Two Daisy Chained ScanIO-300LVs and a UUT

Power LED

The power LED on the ScanIO-300LV should be green under normal operating conditions. The ScanIO-300LV features special circuitry to protect it from inadvertent shorts to power or ground by the user. If the LED is red, a fault has been detected. Cycle power on the ScanIO-300LV to clear the fault.

Setting the Interface Voltage

Before connecting to the boundary-scan controller or the target Unit Under Test (UUT), it is necessary to set the interface voltage. The Adjust rotary switch sets the interface voltage of the TAP and I/O pins to voltages between 1.25V and 3.3V. Use a small screwdriver to set the interface voltage. The voltage appears on the LEDs. The ScanIO-300LV retains the set voltage interface value when powered on and off, however, it is better to check the interface voltage (by viewing the LEDs) before connecting to a target board, as an incorrect voltage setting may damage some targets.

Table 2-1 shows the interface voltage that corresponds to each of the rotary switch positions.

Switch Position	Voltage
0	RESERVED
1	1.25 V
2	1.3 V
3	1.4 V
4	1.5 V
5	1.6 V
6	1.7 V
7	1.8 V
8	1.9 V
9	2.0 V
A	2.2 V
B	2.3 V
C	2.5 V
D	2.8 V
E	3.0 V
F	3.3 V

Table 2-1. ScanIO-300LV Rotary Switch Settings

Setting the Signal Type Option

Before connecting to the boundary-scan controller or the target Unit Under Test (UUT), it is necessary to set the interface type to either single ended signaling with programmable voltage levels (default) or to low voltage differential (LVDS) signal levels. Each pair of connectors can be set to either 'normal' or LVDS compatible based on the front panel DIP switch. Table 2-2 shows the DIP switch settings.

DIP Switch	ON (Up) Position	OFF (Down) Position
1	J1/J2 configured to LVDS	J1/J2 configured to TAP voltage
2	J3/J4 configured to LVDS	J3/J4 configured to TAP voltage
3	J5/J6 configured to LVDS	J5/J6 configured to TAP voltage
4	reserved	reserved
5	reserved	reserved
6	reserved	reserved
7	reserved	reserved
8	reserved	reserved

Table 2-2. ScanIO-300LV DIP Switch Specifications

Connecting to the JTAG Controller

The ScanIO-300LV is connected to the JTAG controller via the 20-pin connector labeled "TAP In". Table 2-3 shows the pin assignment for the TAP In connector. The TAP In connector is the Corelis standard connector and can be connected to the Corelis controllers PCI-1149.1/Turbo + ScanTAP-4 or USB-1149.1/E using a 20-pin to 20-pin 1:1 cable, and can be connected to the other Corelis controllers with the cable provided with them.

Pin	Signal Name	I/O	Description
1	TRST*	In	Test Reset
2	GND		Ground
3	TDI	In	Test Data In
4	GND		Ground
5	TDO	Out	Test Data Out
6	GND		Ground
7	TMS	In	Test Mode Select
8	GND		Ground
9	TCK	In	Test Clock
10	GND		Ground
11	(GPIO1)	In/Out	
12	GND		Ground
13	(GPIO2)	In/Out	
14	GND		Ground
15	(GPIO3)	In/Out	
16	GND		Ground
17	Reserved		
18	Reserved		
19	Reserved		
20	Reserved		

Table 2-3. TAP In Connection List

Target TAP Connection

Connect the target TAP to the TAP Out connector of the ScanIO-300LV. The TAP Out connector has presence detect logic that will detect the UUT board and will include the UUT in the scan chain.

Figure 2-2 shows a diagram of this configuration. If the target system has no boundary-scan logic and no TAP, do not connect anything to TAP Out. Table 2-4 shows the connection list for the TAP Out connector.

Pin	Signal Name	I/O	Description
1	TRST*	Out	Test Reset to UUT scan chain
2	GND		Ground
3	TDI	Out	Test Data Out to UUT scan chain
4	GND		Ground
5	TDO	In	Test Data In from UUT scan chain
6	GND		Ground
7	TMS	Out	Test Mode Select to UUT scan chain
8	GND		Ground
9	TCK	Out	Test Clock to UUT scan chain
10	GND		Ground
11	(GPIO1)	In/Out	
12	GND		Ground
13	(GPIO2)	In/Out	
14	GND		Ground
15	(GPIO3)	In/Out	
16	GND		Ground
17	Reserved		
18	Reserved		
19	Reserved		
20	Reserved		

Table 2-4. TAP Out Connection List

NOTE: All ground pins (2,4,6,8,10,12,14,16) must be connected for proper operation.

Digital I/O Test Connection

Each ScanIO-300LV contains six 60-pin connectors which provide the digital I/O channels used for testing. Each of these 300 channels can be independently programmed as input, output or tri-state (high impedance). To create a test system, these test connectors need to be connected to the unit under test using a set of ribbon cables. If a target is designed, as recommended below, with test access connectors, quick and easy attachment to the ScanIO-300LV can be accomplished by plugging in a few mass-terminated test cables (included). This reduces target signal hookup time to a matter of seconds and is the preferred approach. Figure 2-5 shows how the connectors are numbered.

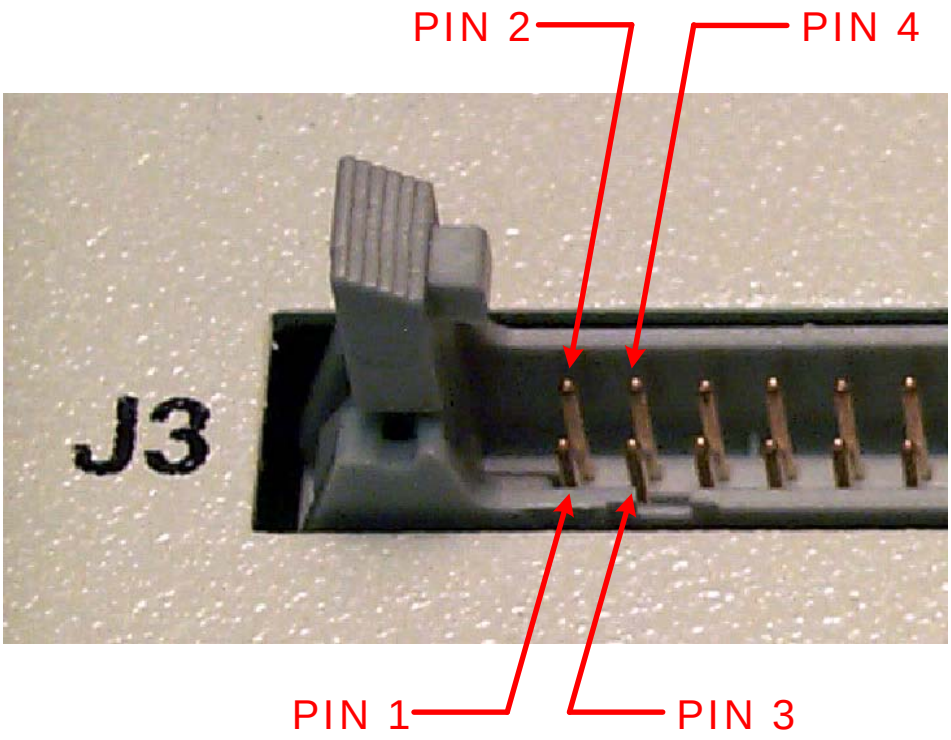

Figure 2-5. 60-pin Connector Pin Numbering

To assist in the building of these cables Table 2-5 shows the pin assignments for connectors J1 to J6.

The function of the pins depends on the mode configuration of the DIP switches. For example, when the I/Os are configured as LVDS, pin 1 would be the positive side of the pair and pin 2 would be the negative side. When in single ended mode, pins 1 and 2 would be separate bi-directional pins.

Pin Number	Single Ended Signal Name	LVDS Signal Name	Pin Number	Single Ended Signal Name	LVDS Signal Name
1	I/O_1	LVDS1_P	2	I/O_2	LVDS1_N
3	I/O_3	LVDS2_P	4	I/O_4	LVDS2_N
5	I/O_5	LVDS3_P	6	I/O_6	LVDS3_N
7	I/O_7	LVDS4_P	8	I/O_8	LVDS4_N
9	I/O_9	**LVDS21_P**	10	GND	GND
11	I/O_11	LVDS5_P	12	I/O_12	LVDS5_N
13	I/O_13	LVDS6_P	14	I/O_14	LVDS6_N
15	GND	GND	16	I/O_16	**LVDS21_N**
17	I/O_17	LVDS7_P	18	I/O_18	LVDS7_N
19	I/O_19	**LVDS22_P**	20	GND	GND
21	I/O_21	LVDS8_P	22	I/O_22	LVDS8_N
23	I/O_23	LVDS9_P	24	I/O_24	LVDS9_N
25	GND	GND	26	I/O_26	**LVDS22_N**
27	I/O_27	LVDS10_P	28	I/O_28	LVDS10_N
29	I/O_29	LVDS23_P	30	GND	GND
31	I/O_31	LVDS11_P	32	I/O_32	LVDS11_N
33	I/O_33	LVDS12_P	34	I/O_34	LVDS12_N
35	GND	GND	36	I/O_36	LVDS23_N
37	I/O_37	LVDS13_P	38	I/O_38	LVDS13_N
39	I/O_39	**LVDS24_P**	40	GND	GND
41	I/O_41	LVDS14_P	42	I/O_42	LVDS14_N
43	I/O_43	LVDS15_P	44	I/O_44	LVDS15_N
45	GND	GND	46	I/O_46	**LVDS24_N**
47	I/O_47	LVDS16_P	48	I/O_48	LVDS16_N
49	I/O_49	**LVDS25_P**	50	GND	GND
51	I/O_51	LVDS17_P	52	I/O_52	LVDS17_N
53	I/O_53	LVDS18_P	54	I/O_54	LVDS18_N
55	I/O_55	LVDS19_P	56	I/O_56	LVDS19_N
57	I/O_57	LVDS20_P	58	I/O_58	LVDS20_N
59	I/O_59	**LVDS25_N**	60	GND	GND

Table 2-5. 60-pin Connectors J1 – J6 Pin Assignment

Mating Connectors

Table 2-6 shows the mating connectors needed to make cables for the JTAG connector and the I/O port connectors. Note that the mating connectors are socket type flat cable connectors, readily available from multiple sources.

Reference	Manufacturer	Part Number	Description
TAP In	3M	3421-6620	20-pin .100 x .100 Wiremount Socket with Strain Relief
TAP Out	3M	3421-6620	20-pin .100 x .100 Wiremount Socket with Strain Relief
J1-J6	3M	3334-6660	60-pin .100 x .100 Wiremount Socket with Strain Relief

Table 2-6. Mating Connectors for the ScanIO-300LV

Chapter 3
Preparation of Test Input Files

Introduction

The ScanIO-300LV integrates easily with a boundary-scan test plan. When the ScanIO-300LV is connected to a socket, the connector behaves like a boundary-scan component. Once the ScanIO-300LV is plugged into the connector on the target board, the boundary-scan test system will automatically test the socket. However, regeneration of the interconnect tests with ScanExpressTPG using the relevant ScanIO-300LV input files is required.

In order to automatically create test vectors for the target UUT that include the ScanIO-300LV connections, the user needs to provide combined UUT + ScanIO-300LV target files:

1. A netlist that contains both the target UUT nets and the relevant ScanIO-300LV pins that are connected to these nets

2. A topology file that also contains the ScanIO-300LV devices

The best, easiest and most straightforward way to prepare the files for the combined target is to use ScanExpress Merge. ScanExpress Merge provides integrated support for the ScanIO and ScanDIMM products. Designating a UUT connector to ScanIO-300LV connection is as easy as point and click from a user friendly GUI selection screen. ScanExpress Merge provides:

- Automatic connection of ScanIO-300LV pins to UUT designated connector pins
- Menu selection of various ScanIO and ScanDIMM modules
- Automatic netlist name prefix addition for ease of use and diagnostics
- Automatic reference designator name prefix addition for ease of use and diagnostics
- User selectable assignment of ScanIO-300LV connector pins to relevant UUT connector pins (1-to-1 or signals only)
- Easy connection customization from intuitive GUI
- Automatic generation of cable(s) connection wirelist(s)
- Allows merging multiple modules, daughter boards, etc. into a single boundary-scan testable entity enabling testing of a complete multiple board assembly as a whole.

All the user needs to do is designate the connectors that they would like to connect to a ScanIO-300LV module and the ScanExpress Merge automatically prepares the relevant netlist and topology files. Additionally, it automatically prepares the suggested cable wiring list which the user can customize and modify from an easy to use GUI function screen.

Using ScanExpress Merge eliminates the need to manually modify netlist and topology files, manually prepare cable wiring lists, and manually edit and rename nets, devices and pins. ScanExpress Merge accommodates seamless board revision and allows re-loading of new netlist(s) into existing designs which is typically required when board revisions are made.

If you are using ScanExpress Merge to prepare the test inputs files, you can skip to the next chapter.

Simplified Example

The remainder of this chapter is provided for clarification only. The following is a simplified example of using the ScanIO-300LV. Note that in this example ScanExpress Merge is not used because the target connector pinout perfectly matches the ScanIO-300LV connector pinout one to one. This example is only brought here in order to provide better understanding of how the ScanIO-300LV files are actually merged with the target UUT file and then used to create test vectors. This simplified example explains the steps necessary to manually merge and test the interconnect of an edge connector to on-board boundary-scan compatible buffers and to non-boundary-scan cluster logic. Figure 3-1 shows a partial schematic for the example given in this chapter.

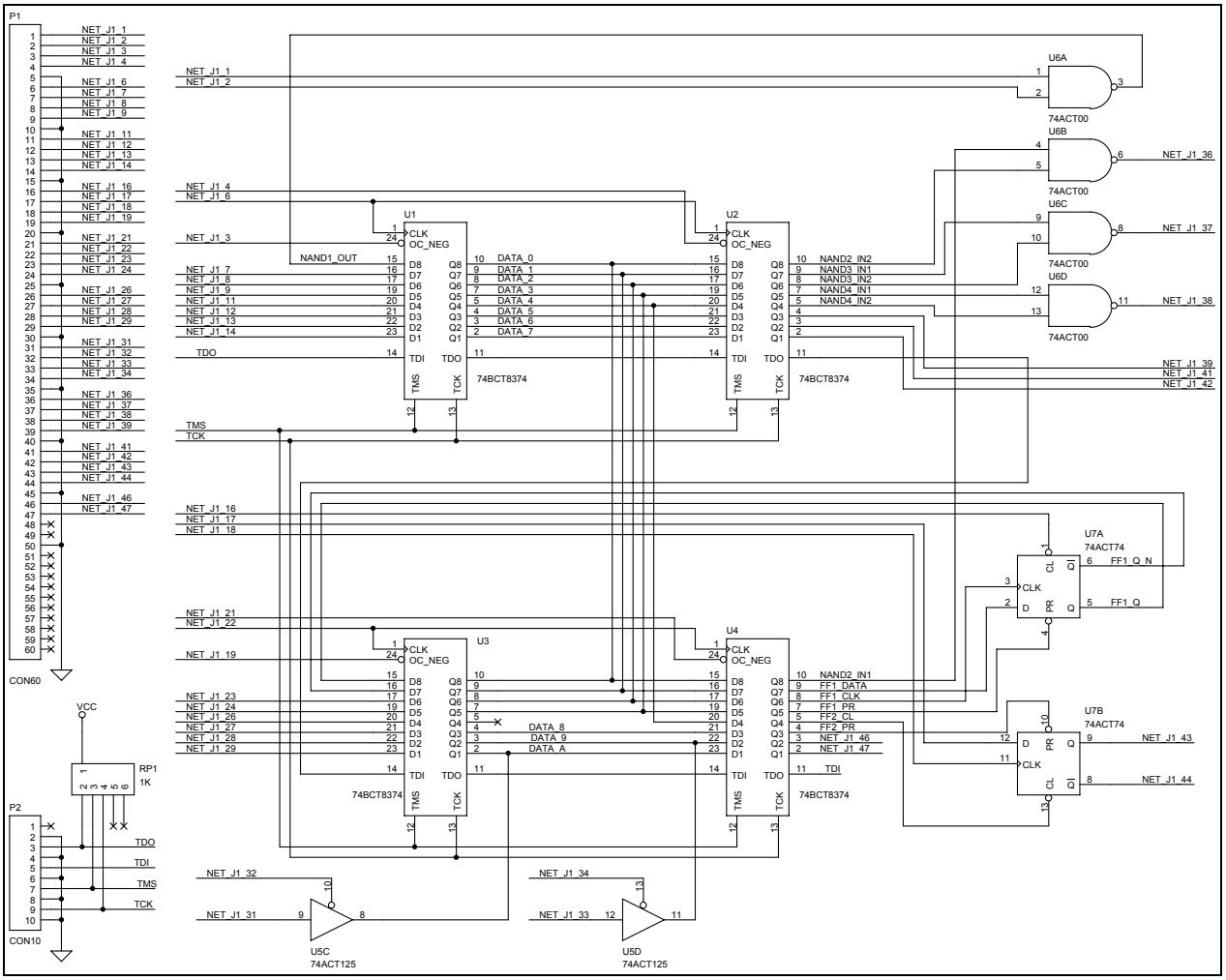

Figure 3-1. Schematic of an Example Unit Under Test

In the example shown in Figure 3-1 above, only nets DATA_0-DATA_8 are fully testable. The outputs from buffers U2 and U4, the inputs to U1 and U3 which connect to either non-boundary-scan logic or the edge connector cannot be tested using boundary-scan techniques under normal circumstances since there is only one boundary-scan cell on each net. With the use of the ScanIO-300LV, the visibility of the boundary-scan chain can be expanded to include these nets.

ScanIO-300LV Interface

Connector P1 on the example schematic is the interface with the ScanIO-300LV. If board space permits, it is recommended to use 60-pin 0.100" x 0.100" connectors with pinouts compatible with the ScanIO-300LV. This allows easy connection with 1:1 cables. The following is the 3M brand part number for the above connector with latch/ejector:

3M Part Number	***Description***
3372-6302	Straight header, 60-pin, 4 wall with center notch

Sometimes the ScanIO-300LV is used to test a particular connector on a design which is not the same connector as used on the ScanIO-300LV. This will work too, the cable is just more complicated.

Generating Test Vectors with ScanExpressTPG

Copy the file ScanIO-300LV.bsd to your design directory. Add the ScanIO-300LV to the topology file and regenerate your test vectors.

Example Topology File

To create a topology file describing the whole system, simply add the boundary-scan components of the ScanIO-300LV to the topology file of the target UUT. In the topology file each ScanIO-300LV connector (J1-J6) takes the reference number of the target connector to which it is connected. How the ScanIO-300LV components are connected to the target system determines the order that they appear in the topology file.

The boundary-scan components on the target board must be added to the DEVICES section of the topology file in order from TDI to TDO. Therefore, the ScanIO-300LV ASICs are added to the topology file in that order. If the ScanIO-300LV unit is connected to TAP2 then the ASICs are placed at the end of the topology file. When a UUT is connected to the ScanIO-300LV via the TAP Out connector, it follows the ScanIO-300 in the boundary-scan chain.

Figure 3-2 is an example of a target system with a ScanIO-300LV unit connected to a second TAP. J1 of the ScanIO-300LV is connected with a 60-pin 1:1 cable to the 60-pin target connector P1. The file shows that the ScanIO-300LV contains six boundary-scan devices in order from TDI to TDO that are referenced as P1 and ASIC2-ASIC6. These six devices are described by BSDL file SCANIO-300LV.BSD.

```
!-------------------------------------------------------------------
! TOPOLOGY FILE
!-------------------------------------------------------------------
! Filename  : Scanio&JDB.top
! Created on: 8/24/2005
!
! Boundary-Scan topology file for the ScanIO-300 & JDB
!-------------------------------------------------------------------

!-------------------------------------------------------------------
! TAP #1
!-------------------------------------------------------------------

CHAIN Chain1
    DEVICES

   !------    -------------------    -------    ------
   !DEVICE    BSDL FILENAME          PACKAGE    BYPASS
   !------    -------------------    -------    ------
    U1        "74BCT8374"            DW_PACKAGE NO
    U2        "74BCT8374"            DW_PACKAGE NO
    U3        "74BCT8374"            DW_PACKAGE NO
    U4        "74BCT8374"            DW_PACKAGE NO

    END_DEVICES
END_CHAIN

!-------------------------------------------------------------------
! TAP #2
!-------------------------------------------------------------------

CHAIN Chain2
    DEVICES

   !------    -------------------    -------    ------
   !DEVICE    BSDL FILENAME          PACKAGE    BYPASS
   !------    -------------------    -------    ------
    P1        "ScanIO-300LV.bsd"     PIN60      NO
    ASIC2     "ScanIO-300LV.bsd"     PIN60      NO
    ASIC3     "ScanIO-300LV.bsd"     PIN60      NO
    ASIC4     "ScanIO-300LV.bsd"     PIN60      NO
    ASIC5     "ScanIO-300LV.bsd"     PIN60      NO
    ASIC6     "ScanIO-300LV.bsd"     PIN60      NO

    END_DEVICES
END_CHAIN
```

Figure 3-2. Example Topology File

Creating Test Vectors

The files necessary for creating example boundary-scan tests are installed by the ScanExpress installer in the directory "ScanIO-300LV/Example". An explanation of this is beyond the scope of this User's Manual but can be found in the Corelis ScanExpressTPG User's Manual.

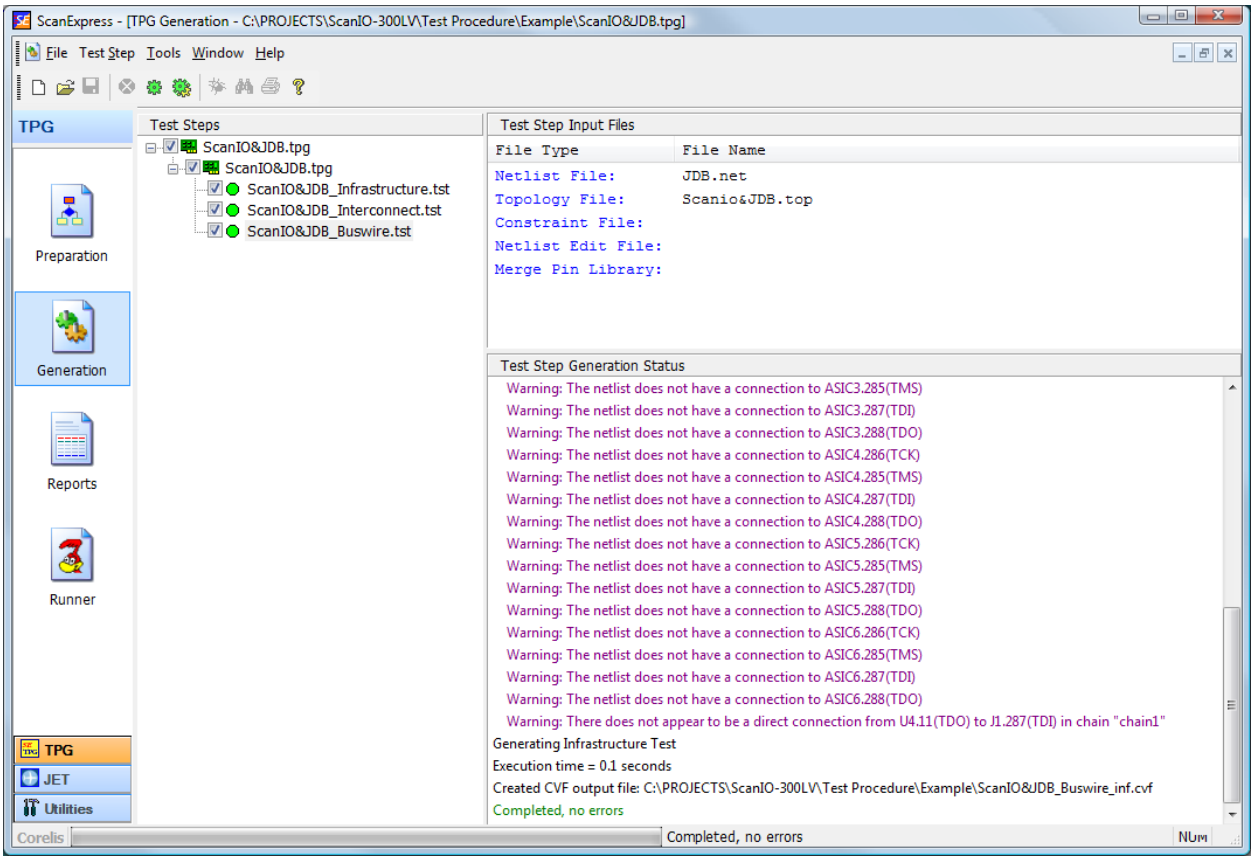

Figure 3-3. ScanExpressTPG Test Step

Appendix A
Related Software

What's on the Disk

The files related to the ScanIO-300LV are installed by the ScanExpress installer.

Filename	Description
ScanIO-300LV.bsd	BSDL file for the ScanIO-300LV boundary-scan components
ScanIO-300LV_LVDS.bsd	BSDL file for the ScanIO-300LV boundary-scan components in LVDS mode
\Example\74bct8374	BSDL file for SN74BCT8374 boundary-scan chips on example Unit Under Test
\Example\ScanIO-300LV.bsd	BSDL file for the ScanIO-300LV boundary-scan components
\Example\JDB.net	Telesis format netlist of example UUT.
\Example\Scanio&JDB.edt	Netlist edit file for example UUT and ScanIO-300LV
\Example\Scanio&JDB.top	Topology file showing scan chain for example UUT and ScanIO-300LV
\Selftest\ScanIO-300LV_Selftest.tsp	ScanExpress Runner test plan file for the selftest boundary-scan vectors
\Selftest\ScanIO-300LV_Selftest_infrastructure_inf.cvf	Selftest infrastructure test vector file
\Selftest\ScanIO-300LV_Selftest_interconnect_ic.cvf	Selftest interconnect test vector file. Requires Corelis ScanExpress Runner to execute test. Must connect 60 pin 1:1 cables from J1 to J2, from J3 to J4, and from J5 to J6.
\Selftest\ScanIO-300LV_Selftest_buswire_bus.cvf	Selftest buswire test vector file. Requires Corelis ScanExpress Runner to execute test. Must connect 60 pin 1:1 cables from J1 to J2, from J3 to J4, and from J5 to J6.

Executing Self Test with ScanExpress Runner

The ScanIO-300LV comes with three compact vector format self test files, ScanIO-300LV_Selftest_infrastructure_inf.cvf, ScanIO-300LV_Selftest_interconnect_ic.cvf and ScanIO-300LV_Selftest_buswire_bus.cvf. In order to execute these files, you need Corelis ScanExpress Runner test execution software and a Corelis Boundary-Scan controller such as the PCI-1149.1/Turbo or USB-1149.1/E with a 20-pin TAP cable. To complete all three tests, three-sixty pin 1:1 cables are necessary to provide loopback on the digital I/O signals.

The infrastructure test verifies that a good TAP connection is being made between the controller and the ScanIO-300LV. It also verifies that the boundary-scan infrastructure of the six ASICs on the ScanIO-300LV is fully functional.

The interconnect and buswire tests verify that all 300 digital I/Os of the ScanIO-300LV are fully functional. These tests are completed without a target attached. To test all of the I/Os, three 60-pin 1:1 cables must be connected between connector pairs J1 and J2, J3 and J4, and J5 and J6. Note that this test not only tests the ScanIO-300LV digital I/Os but also tests the connectivity of the 60-pin 1:1 cables. If you are using 60-pin 1:1 cables to connect to your target, this is a good way to verify that the cables are good.

Running the Infrastructure, Interconnect and Buswire Tests

Using ScanExpress Runner, follow the steps below to load and run a ScanIO-300LV self test on your computer. The self test consists of Infrastructure, Interconnect and Buswire tests between pairs of ScanIO-300LV connectors which are connected to each other using the supplied 60-pin 1:1 cables:

Step 1 Connect the 5V power supply to the ScanIO-300LV.

Step 2 Make sure no target is connected to the ScanIO-300LV, then power it up by turning on the Power switch.

Step 3 Set the interface voltage by using a screwdriver to rotate the adjust switch. All three self test steps can be run at any voltage.

Step 4 Set the DIP switch to the all OFF position.

Step 5 Connect one end of the 20-pin TAP cable to the boundary-scan controller and the other end to the TAP In connector on the ScanIO-300LV.

Step 6 Connect a 60-pin 1:1 cable between J1 and J2. Connect another 60-pin 1:1 cable between J3 and J4. Connect another 60-pin 1:1 cable between J5 and J6.

Step 7 Double-click on the ScanExpress Runner icon to bring up the ScanExpress Runner main screen.

Step 8 From the menu, select **File**, then **Open Test Plan**.

Step 9 Browse to the file "ScanIO-300LV_Selftest.tsp" and click **OK**.

Step 10 From the main menu, select **Setup**, then **Controller,** then select the boundary-scan controller that you are using and set its TCK frequency option to 10MHz. Set the controller voltage option to the interface voltage chosen in step 3.

Step 11 Select **Run Test**. The test should run and pass. Figure A-1 shows the three passing self test steps.

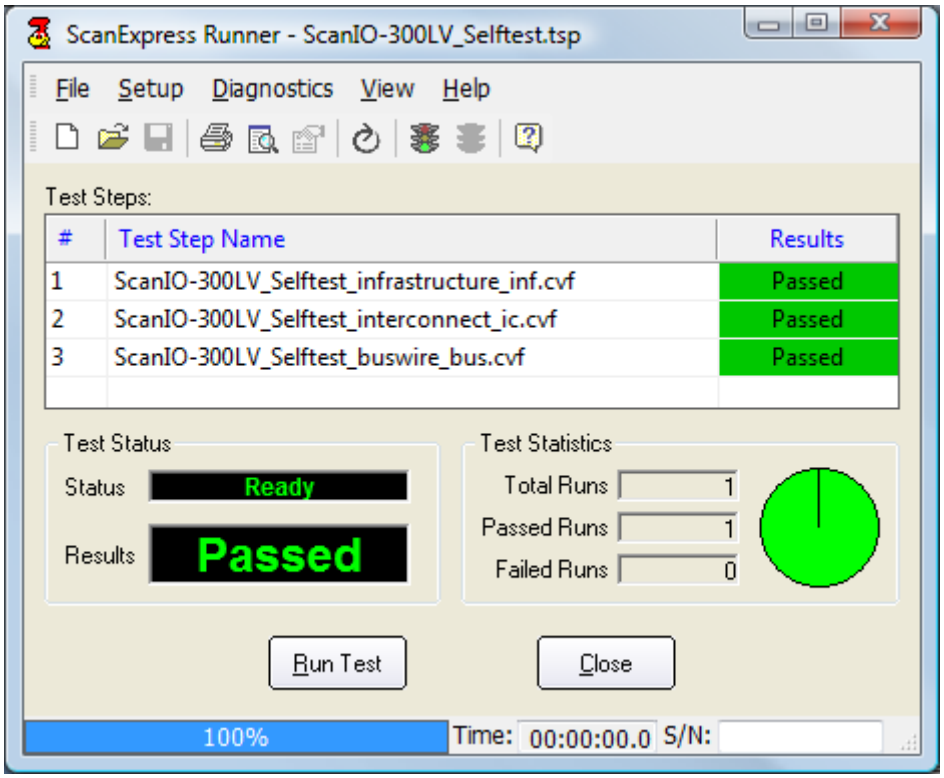

Figure A-1. ScanExpress Runner Self Test

Appendix B
Target TAP Design

The TAP contains 5 signals: TCK, TMS, TDO, TDI and optionally TRST*. It also contains ground signal(s). The Corelis recommended standard TAP connector is shown in Figure B-1 and is widely regarded as the industry standard. Note that each signal is terminated with resistor in order to minimize signal cross-talk in the interface cable and maximize noise immunity.

The connector on the user's target should have the standard flat cable compatible pinout. Below is the top view of the target 20-pin connector header (0.100" x 0.100" spacing):

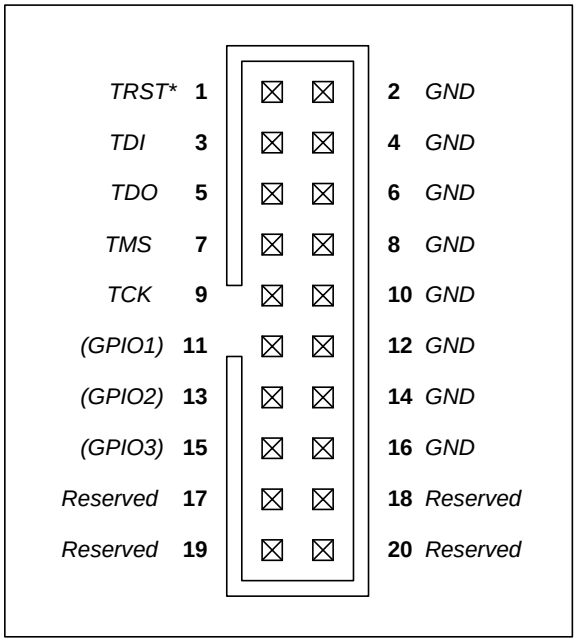

Figure B-1. Standard 20-pin TAP Connector (top view)

The following are two 3M brand part numbers for the above connector. Both are 0.100" x 0.100" headers, one with and one without a latch/ejector. Note that there are many other manufacturers who would have similar parts as well:

3M Part Number	***Description***
30320-6002HB	Straight header, 20-pin, 4 wall, with center notch
3428-6302	Latch/Ejector Straight header, 20-pin, 4 wall, with notch

Target TAP Schematics

The typical schematics of the target TAP connector and the recommended termination resistors are shown in Figure B-2. The 1K pull-up resistors can be connected to any Vcc supply with nominal voltage between 1.25V to 3.3V. Recommended resistor values are +/- 5%.

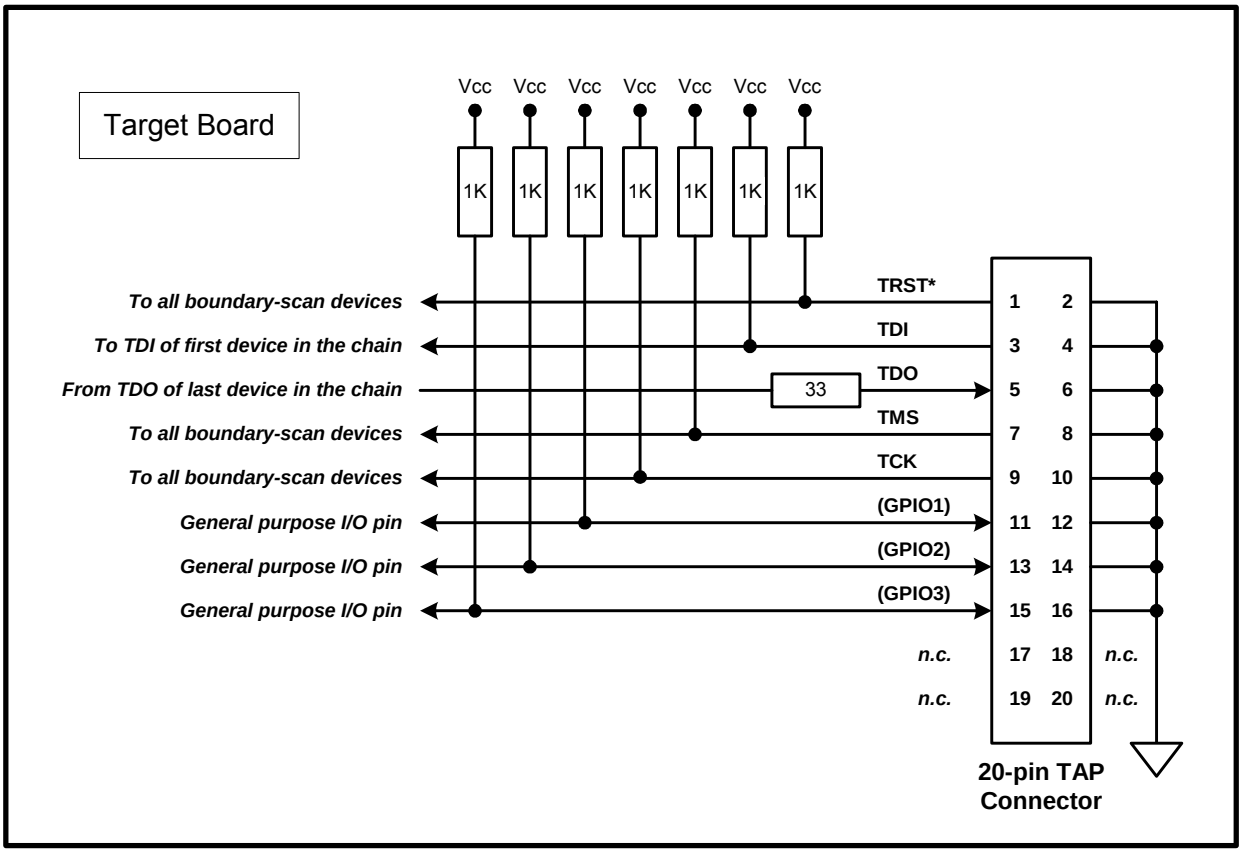

Figure B-2. 20-pin TAP Connector Schematics

Please refer to Corelis application note 03-304 for additional details on the different target connector formats.