JTAG Applications

While it is obvious that JTAG based testing can be used in the production phase of a product, new developments and applications of the IEEE-1149.1 standard have enabled the use of JTAG in many other product life cycle phases. Specifically, JTAG technology is now applied to product design, prototype debugging and field service as depicted in Figure 1. This means the cost of the JTAG tools can be amortized over the entire product life cycle, not just the production phase.

Product Life-Cycle Support

To facilitate this product life cycle concept, JTAG tool vendors such as Corelis offer an integrated family of software and hardware solutions for all phases of a product’s life-cycle. All of these products are compatible with each other, thus protecting the user’s investment.

Applying JTAG for Product Development

The ongoing marketing drive for reduced product size, such as portable phones and digital cameras, higher functional integration, faster clock rates, and shorter product life-cycle with dramatically faster time-to-market has created new technology trends. These trends include increased device complexity, fine pitch components, such as surface-mount technology (SMT), systems-in-package (SIPs), multi-chip modules (MCMs), ball-grid arrays (BGAs), increased IC pin-count, and smaller PCB traces. These technology advances, in turn, create problems in PCB development:

- Many boards include components that are assembled on both sides of the board. Most of the through-holes and traces are buried and inaccessible.
- Loss of physical access to fine pitch components, such as SMTs and BGAs, makes it difficult to probe the pins and distinguish between manufacturing and design problems.
- Often a prototype board is hurriedly built by a small assembly shop with lower quality control as compared to a production house. A prototype generally will include more assembly defects than a production unit.
- When the prototype arrives, a test fixture for the ICT is not available and, therefore, manufacturing defects cannot be easily detected and isolated.
- Small-size products do not have test points, making it difficult or impossible to probe suspected nodes.
- Many Complex Programmable Logic Devices (CPLDs) and flash memory devices (in BGA packages) are not socketed and are soldered directly to the board.
- Every time a new processor or a different flash device is selected, the engineer has to learn from scratch how to program the flash memory.
- When a design includes CPLDs from different vendors, the engineer must use different in-circuit programmers to program the CPLDs.

JTAG technology is the only cost-effective solution that can deal with the above problems. In recent years, the number of devices that include JTAG has grown dramatically. Almost every new microprocessor that is being introduced includes JTAG circuitry for testing and in-circuit emulation. Most of the CPLD and field programmable array (FPGA) manufacturers, such as Altera, Lattice and Xilinx, to mention a few, have incorporated JTAG logic into their components, including additional circuitry that uses the JTAG four-wire interface to program their devices in-system.

As the acceptance of JTAG as the main technology for interconnect testing and in-system programming (ISP) has increased, the various JTAG test and ISP tools have matured as well. The increased number of JTAG components and mature JTAG tools, as well as other factors that will be described later, provide engineers with the following benefits:
- Easy to implement Design-For-Testability (DFT) rules. A list of basic DFT rules is provided later in this article.
- Design analysis prior to PCB layout to improve testability.
- Packaging problems are found prior to PCB layout.
- Little need for test points.
- No need for test fixtures.
- More control over the test process.
- Quick diagnosis (with high resolution) of interconnection problems without writing any functional test code.
- Program code in flash devices.
- Design configuration data placement into CPLDs.
- JTAG emulation and source-level debugging.

What JTAG Tools are needed?

In the previous section, we listed many of the benefits that a designer enjoys when incorporating boundary-scan in his product development. In this section we describe the tools and design data needed to develop JTAG test procedures and patterns for ISP, followed by a description of how to test and program a board. We use a typical board as an illustration for the various JTAG test functions needed. A block diagram of such a board is depicted in Figure 2.

A typical digital board with JTAG devices includes the following main components:

- Various JTAG components such as CPLDs, FPGAs, Processors, etc., chained together via the boundary-scan path.
- Non-JTAG components (clusters).
- Various types of memory devices.
- Flash Memory components.
- Transparent components such as series resistors or buffers.

Most of the boundary-scan test systems are comprised of two basic elements: Test Program Generation and Test Execution. Generally, a Test Program Generator (TPG) requires the netlist of the Unit Under Test (UUT) and the BSDL files of the JTAG components. The TPG automatically generates test patterns that allow fault detection and isolation for all JTAG testable nets of the PCB. A good TPG can be used to create a thorough test pattern for a wide range of designs. For example, ScanExpress TPG typically achieves net coverage of more than 60%, even though the majority of the PCB designs are not optimized for boundary-scan testing. The TPG also creates test vectors to detect faults on the pins of non-scannable components, such as clusters and memories that are surrounded by scannable devices.

Some TPGs also generate a test coverage report that allows the user to focus on the non-testable nets and determine what additional means are needed to increase the test coverage.
Test programs are generated in seconds. For example, when Corelis ScanExpress TPG™ was used, it took a 3.0 GHz Pentium 4 PC 23 seconds to generate an interconnect test for a UUT with 5,638 nets (with 19,910 pins). This generation time includes netlist and all other input files processing as well as test pattern file generation.

Test execution tools from various vendors provide means for executing JTAG tests and performing in-system programming in a pre-planned specific order, called a test plan. Test vectors files, which have been generated using the TPG, are automatically applied to the UUT and the results are compared to the expected values. In case of a detected fault, the system diagnoses the fault and lists the failures as depicted in Figure 3. Figure 3 shows the main window of the Corelis test execution tool, ScanExpress Runner™. ScanExpress Runner gives the user an overview of all test steps and the results of executed tests. These results are displayed both for individual tests as well as for the total test runs executed. ScanExpress Runner provides the ability to add or delete various test steps from a test plan, or re-arrange the order of the test steps in a plan. Tests can also be enabled or disabled

Different test plans may be constructed for different UUTs. Tests within a test plan may be re-ordered, enabled or disabled, and unlimited different tests can be combined into a test plan. ScanExpress Runner can be used to develop a test sequence or test plan from various independent sub-tests. These sub-tests can then be executed sequentially as many times as specified or continuously if desired. A sub-test can also program CPLDs and flash memories. For ISP, other formats, such as SVF, JAM, and STAPL, are also supported.

To test the board depicted in Figure 2, the user must execute a test plan that consists of various test steps as shown in Figure 3.

The first and most important test is the scan chain infrastructure integrity test. The scan chain must work correctly prior to proceeding to other tests and ISP. Following a successful test of the scan chain, the user can proceed to testing all the interconnections between the JTAG components. If the interconnect test fails, ScanExpress Runner displays a diagnostic screen that identifies the type of failure (such as stuck-at, Bridge, Open) and lists the failing nets and pins as shown in Figure 4. Once the interconnect test passes, including the testing of transparent components, it makes sense to continue testing the clusters and the memory devices. At this stage, the system is ready for in-system programming, which typically takes more time as compared to testing.
During the design phase of a product, some JTAG vendors will provide design assistance in selecting JTAG-compliant components, work with the developers to ensure that the proper BSDL files are used, and provide advice in designing the product for testability.

### Applying JTAG for Production Test

Production testing, utilizing traditional In-Circuit Testers that do not have JTAG features installed, experience similar problems that the product developer had and more:

- Loss of physical access to fine pitch components, such as SMTs and BGAs, reduces bed-of-nails ICT fault isolation.
- Development of test fixtures for ICTs becomes longer and more expensive.
- Development of test procedures for ICTs becomes longer and more expensive due to more complex ICs.
- Designers are forced to bring out a large number of test points, which is in direct conflict with the goal to miniaturize the design.
- In-system programming is inherently slow, inefficient, and expensive if done with an ICT.
- Assembling boards with BGAs is difficult and subject to numerous defects, such as solder smearing.

### JTAG Embedded Functional Test

Recently, a test methodology has been developed which combines the ease-of-use and low cost of boundary-scan with the coverage and security of traditional functional testing. This new technique, called JTAG Emulation Test (JET), lets engineers automatically develop PCB functional test that can be run at full speed. If the PCB has an on-board processor with a JTAG port (common, even if the processor doesn’t support boundary-scan), JET and boundary-scan tests can be executed as part of the same test plan to provide extended fault coverage to further complement or replace ICT testing.

Corelis ScanExpress JET™ provides JTAG embedded test for a wide range of processors. For more information about this technology and product, visit the ScanExpress JET product page.

### Production Test Flow

Figure 5 shows different production flow configurations. The diagram shows two typical ways that JTAG is deployed:

- As a stand-alone application at a separate test station or test bench to test all the interconnects and perform ISP of on-board flash and other memories. JTAG embedded functional test (JET) may be integrated with boundary-scan.
- Integrated into the ICT system, where the JTAG control hardware is embedded in the ICT system and the boundary-scan (and possibly JET) software is a module called from the ICT software system.

In the first two cases, the test flow is sometimes augmented with a separate ICT stage after the JTAG-based testing is completed, although it is becoming more common for ICT to be skipped altogether or at least to be limited to analog or special purpose functional testing.

Figure 5. Typical Production Flows
The following are major benefits in using JTAG test and in-system programming in production:

- No need for test fixtures.
- Integrates product development, production test, and device programming in one tool/system.
- Engineering test and programming data is reused in Production.
- Fast test procedure development.
- Preproduction testing can start the next day when prototype is released to production.
- Dramatically reduces inventory management – no pre-programmed parts eliminates device handling and ESD damage.
- Eliminates or reduces ICT usage time – programming and screening.

Production test is an obvious area in which the use of boundary-scan yields tremendous returns. Automatic test program generation and fault diagnostics using JTAG software products and the lack of expensive fixturing requirements can make the entire test process very economical. For products that contain edge connectors and digital interfaces that are not visible from the boundary-scan chain, JTAG vendors offer a family of boundary-scan controllable I/Os that provide a low cost alternative to expensive digital pin electronics.

Field Service and Installation

The role of JTAG does not end when a product ships. Periodic software and hardware updates can be performed remotely using the boundary-scan chain as a non-intrusive access mechanism. This allows flash updates and reprogramming of programmable logic, for example. Service centers that normally would not want to invest in special equipment to support a product now have an option of using a standard PC or laptop for JTAG testing. A simple PC-based JTAG controller can be used for all of the above tasks and also double as a fault diagnostic system, using the same test vectors that were developed during the design and production phase. This concept can be taken one step further by allowing an embedded processor access to the boundary-scan chain. This allows diagnostics and fault isolation to be performed by the embedded processor. The same diagnostic routines can be run as part of a power-on self-test procedure.

JTAG Design-for-Test Basic Considerations

As mentioned earlier in this article, the design for JTAG test guidelines are simple to understand and follow compared to other traditional test requirements. It is important to remember that JTAG testing is most successful when the design and test engineering teams work together to ensure that testability is “designed in” from the start. The boundary-scan chain is the most critical part of JTAG implementations. When that is properly implemented, improved testability inevitably follows.

Below is a list of basic guidelines to observe when designing a JTAG-testable board:

- If there are programmable components in a chain, such as FPGAs, CPLDs, etc., group them together in the chain order and place the group at either end of the chain. It is recommended that you provide access to Test Data In (TDI) and Test Data Out (TDO) signals where the programmable group connects to the non-programmable devices.
- All parts in the boundary-scan chain should have 1149.1-compliant test access ports (TAPs).
- Use simple buffering for the Test Clock (TCK) and Test Mode Select (TMS) signals to simplify test considerations for the boundary-scan TAP. The TAP signals should be buffered to prevent clocking and drive problems.
- Group similar device families and have a single level converter interface between them, TCK, TMS, TDI, TDO, and system pins.
- TCK should be properly routed to prevent skew and noise problems.
- Use the standard JTAG connector on your board as depicted in Corelis documentation.
- Ensure that BSDL files are available for each JTAG component that is used on your board and that the files are validated.
Design for interconnect testing requires board-level system understanding to ensure higher test coverage and elimination of signal level conflicts.

- Determine which JTAG components are on the board. Change as many non-JTAG components to IEEE 1149.1-compliant devices as possible in order to maximize test coverage.

- Check non-JTAG devices on the board and design disabling methods for the outputs of those devices in order to prevent signal level conflicts. Connect the enable pins of the conflicting devices to JTAG controllable outputs. Corelis tools will keep the enable/disable outputs at a fixed disabling value during the entire test.

- Ensure that your memory devices are surrounded by JTAG components. This will allow you to use a test program generator, such as ScanExpress TPG, to test the interconnects of the memory devices.

- Check the access to the non-boundary-scan clusters. Make sure that the clusters are surrounded by JTAG components. By surrounding the non-boundary-scan clusters with JTAG devices, the clusters can then be tested using a JTAG test tool.

- If your design includes transparent components, such as series resistors or non-inverting buffers, your test coverage can be increased by testing through these components using ScanExpress TPG.

- Connect all I/Os to JTAG controllable devices. This will enable the use of JTAG, digital I/O module, such as the ScanIO-300LV, to test all your I/O pins, thus increasing test coverage.