What is JTAG?

Introduction

Since its introduction as an industry standard in 1990, JTAG has continuously grown in adoption, popularity, and usefulness—even today, new revisions and supplements to the IEEE-1149.1 standard are being developed and implemented. This document is a brief introduction to the nature and history of JTAG, from its introduction to new extensions in current development.

What is JTAG?

JTAG, commonly referred to as boundary-scan and defined by the Institute of Electrical and Electronic Engineers (IEEE) 1149.1, originally began as an integrated method for testing interconnects on printed circuit boards (PCBs) implemented at the integrated circuit (IC) level. As PCBs grew in complexity and density—a trend that continues today—limitations in the traditional test methods of in-circuit testers (ICTs) and bed of nails fixtures became evident. Packaging formats, specifically Ball Grid Array (BGA, depicted in Figure 1) and other fine pitch components, designed to meet ever-increasing physical space constraints, also led to a loss of physical access to signals.

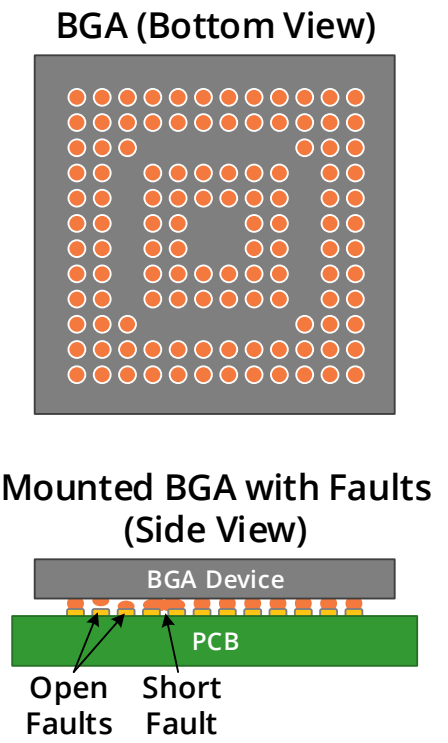

Figure 1. BGA faults are difficult to detect and diagnose without JTAG.

These new technology developments led to dramatic increases in costs related to designing and building bed of nails fixtures; at the same time, circuit board test coverage also suffered. JTAG/boundary-scan presented an elegant solution to this problem: build functionality into the IC to assist in testing assembled electronic systems.

Today, JTAG is used for everything from testing interconnects and functionality on ICs to programming flash memory of systems deployed in the field and everything in-between. JTAG and its related standards have been and will continue to be extended to address additional challenges in electronic test and manufacturing, including test of 3D ICs and complex, hierarchical systems.

History of JTAG

In the 1980s, the Joint Test Action Group (JTAG) set out to develop a specification for boundary-scan testing that was standardized in 1990 as the IEEE Std. 1149.1-1990. A few years later in 1993, a new revision to the standard—1149.1a—was introduced to clarify, correct, and enhance the original specification. An additional supplement, 1149.1b, was published in 1994 to add Boundary-Scan Description Language (BSDL) to the standard, paving the way for fast, automated test development and spurring continuous adoption by major electronics producers all over the world. The lessons that were learned became formalized in an update to the core standard in 2001 and IEEE-1149.1-2001 was published.

As new applications of JTAG were discovered, new standards were developed to extend the capabilities of JTAG. Standards such as the IEEE-1149.5 module test and maintenance bus standard in 1995 and the IEEE-1149.4 standard for mixed-signal testing in 1999 were met with low adoption rates and are not widely used at present. The IEEE-1149.6 standard introduced in 2003, on the other hand, began with slow adoption but has since become standard in many ICs as the technology it addressed—high-speed, AC-coupled signals—became a common feature of electronic systems. IEEE-1149.7, published in 2009 to address the need for JTAG in low-pin-count systems, is now standard on many popular microcontrollers.

Additional standards have also been published to add specific test capabilities. In 2002, the IEEE-1532 standard for in-system configuration of programmable devices was released and is now a common feature of FPGAs and their supporting software systems. IEEE-1581 was developed in 2011 to provide a convenient method of testing interconnects of high-speed memories with slow-speed test vectors; a version of this capability is implemented in some DDR4 memory components. To address the

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new application of combined capacitive sensing and boundary-scan test, IEEE-1149.8.1 was published in 2012. The extensibility of JTAG has been proven time and again.

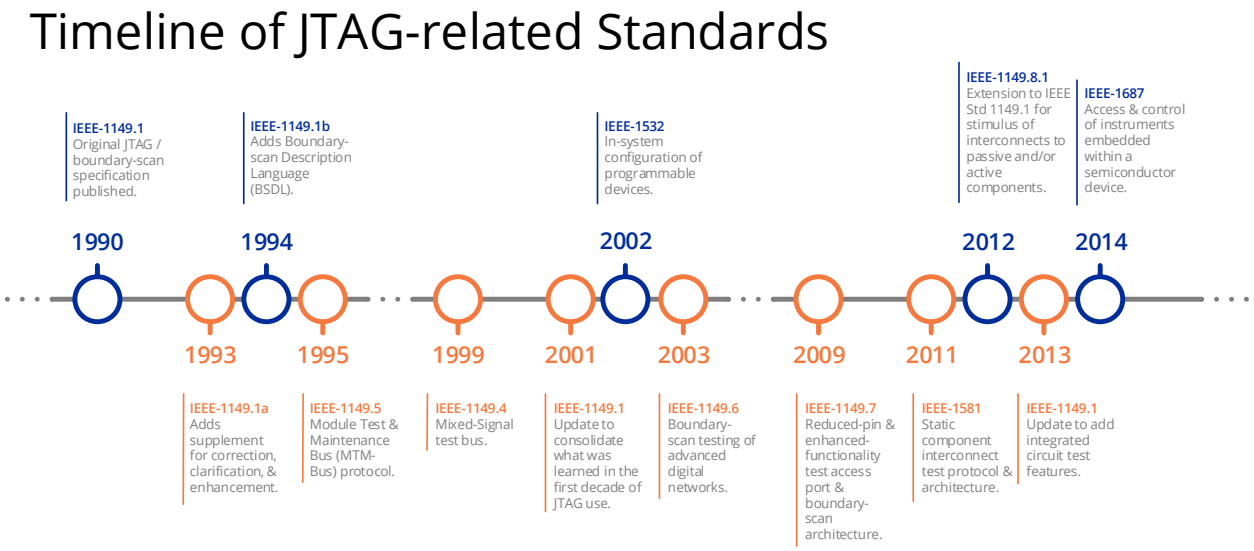

Figure 2. JTAG has been under continuous development for more than 20 years.

More recently, efforts have been made to standardize JTAG access to instruments embedded within ICs. The IEEE-1149.1 standard was updated once more in 2013 for some housekeeping and to add extensions to access these instruments. Just one year later, an alternative standard for accessing these instruments, IEEE-1687, was published. Looking to the future, industry activities to extend JTAG into 3D-IC testing, system-level testing, and high-speed testing are already underway, proving that the versatility and extensibility of JTAG is here to stay.

How JTAG Works

The JTAG/boundary-scan test architecture was originally developed as a method to test interconnects between ICs mounted on a PCB without using physical test probes. Boundary-scan cells created using multiplexer and latch circuits are attached to each pin on the device. These cells, embedded in the device, can capture data from pin or core logic signals as well as force data onto pins. Captured data is serially shifted out through the JTAG Test Access Port (TAP) and can be compared to expected values to determine a pass or fail result. Forced test data is serially shifted into the boundary-scan cells. All of this is controlled from a serial data path called the scan path or scan chain.

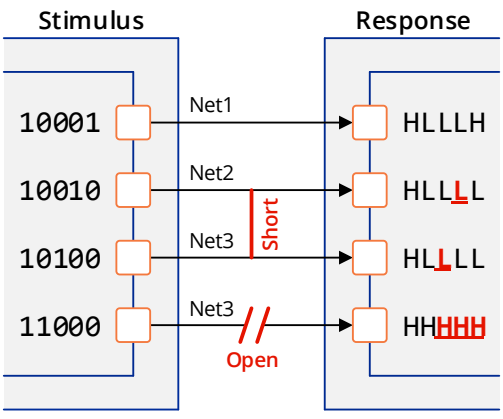

Figure 3. Basic principles of an interconnect test.

Because each pin can be individually controlled, boundary-scan eliminates a large number of test vectors that would normally needed to properly initialize sequential logic. Using JTAG, tens or hundreds of test vectors may do the job that had previously required thousands. Boundary-scan enables shorter test times, higher test coverage, increased diagnostic capability, and lower capital equipment cost.

The principles of interconnect test using boundary-scan components are illustrated in Figure 3. Two boundary-scan compliant devices are connected with four nets. The first device includes four outputs that are driving the four inputs of the other with predefined values. In this case, we assume that the circuit includes two faults: a short fault between Net2 and Net3, and an open fault on Net4. We will also assume that a short between two nets behaves as a wired-AND and an open fault behaves as a stuck-at-1 condition.

To detect and isolate defects, the tester shifts the patterns shown in Figure 3 into the first boundary-scan register and applies these patterns to the inputs of the second device. The input values captured in the

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boundary-scan register of the second device are shifted out and compared to the expected values. In this case, the results, underlined and marked in red on Net2, Net3, and Net4, do not match the expected values and the tester tags these nets as faulty. Sophisticated algorithms are used to automatically generate the minimal set of test vectors to detect, isolate, and diagnose faults to specific nets, devices, and pins.

Of course, interconnect testing is just one of many uses of JTAG—the aforementioned JTAG TAP has been extended to support additional capabilities including in-system-programming (ISP), in-circuit-emulation (ICE), embedded functional testing, and many more. The standard accounts for the addition of device-specific instructions and registers that can be used to interact with additional IC capabilities. For example, a microprocessor device may have embedded functionality for data download, program execution, or register peek-and-poke activities accessible using JTAG TAP; using the same tools, FPGA and CPLD devices can be erased, configured, read-back, and controlled using JTAG instructions through the IEEE-1532 standard. More recently, embedded IC instrumentation—from instruments that measure voltage and current to devices that can execute high-speed test on the chip—has used the JTAG TAP as the access mechanism, providing new visibility into the IC and further expanding the scope of JTAG testing.

Product Life-Cycle Phases and Applications

While JTAG/boundary-scan was originally regarded as a method to test electronic products during the production phase, new developments and applications of the IEEE-1149.1 standard have enabled the use of JTAG in many other product life cycle phases. Boundary-scan technology is commonly applied to product design, prototype debugging, and field service as depicted in Figure 4.

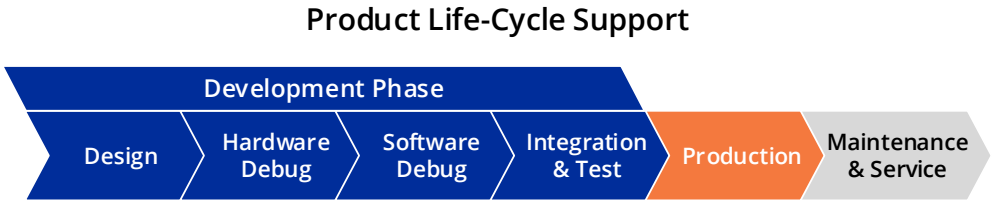

Figure 4. JTAG tools are used in all phases of the product life cycle.

The same test suite used to validate design testability can adapted and utilized for board bring-up, high-volume manufacturing test, troubleshooting and repairs, and even field service and reprogramming. The versatility of JTAG/boundary-scan tools delivers immense value to organizations beyond the production phase.

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